AU526x – Low Noise PLL Based Crystal Oscillator

General Description

The AU526x family of parts is a PLL based crystal oscillator programmable for various output frequencies. The device is user programmable via I2C to provide any frequency between 200KHz to 1GHz. AU526x is a low Noise PLL with Integrated XTAL which provides clocks with Jitter of 110fs(AU5260- Low Jitter) and 85fs(AU5265- Ultra Low Jitter).

AU526x is factory-configurable for a wide variety of user specifications including the I2C address, output format, and OE pin location/polarity .With on chip NVM and factory programming, Aurasemi can satisfy customer requirements with very fast lead times.

Applications:

- 100G/200G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Datacenter
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

Features

- I2C programmable to any frequency from 200KHz to 1 GHz.
- Low Jitter : AU5260 110fs Typ Jrms
  Ultra Low Jitter: AU5265 85fs Typ Jrms
  (12 kHz – 20 MHz)
- Fractional N fully integrated PLL
- 3.3 V, 2.5 V and 1.8 V VDD supply operation
- I2C Interface supports Standard(100 KHz) and Fast Mode(400 KHz)
- Best in class PSRR performance of -85dBC typical
- Output Driver options: LVPECL, LVDS, HCSL-LP, LVDS-Boost, HCSL,CML.
- +/- 25 ppm stability (-40 °C to 85 °C)
- Package Options: Available in 6pin Plastic Package
  - 5 mm x 3.2 mm
  - 3.2 mm x 2.5 mm
  - 5 mm x 7 mm (Contact Aurasemi)
  - 2 mm x 2.5 mm (Contact AuraSemi)

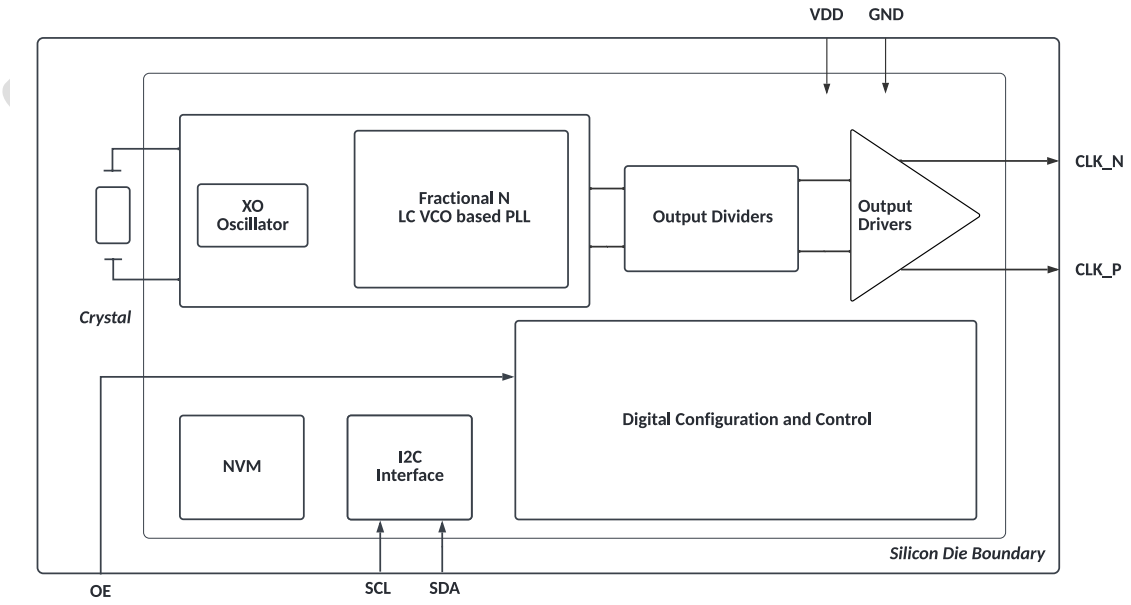


Figure 1 Functional Overview

Table of Contents

List of Tables

List of Figures

1 Pin Description

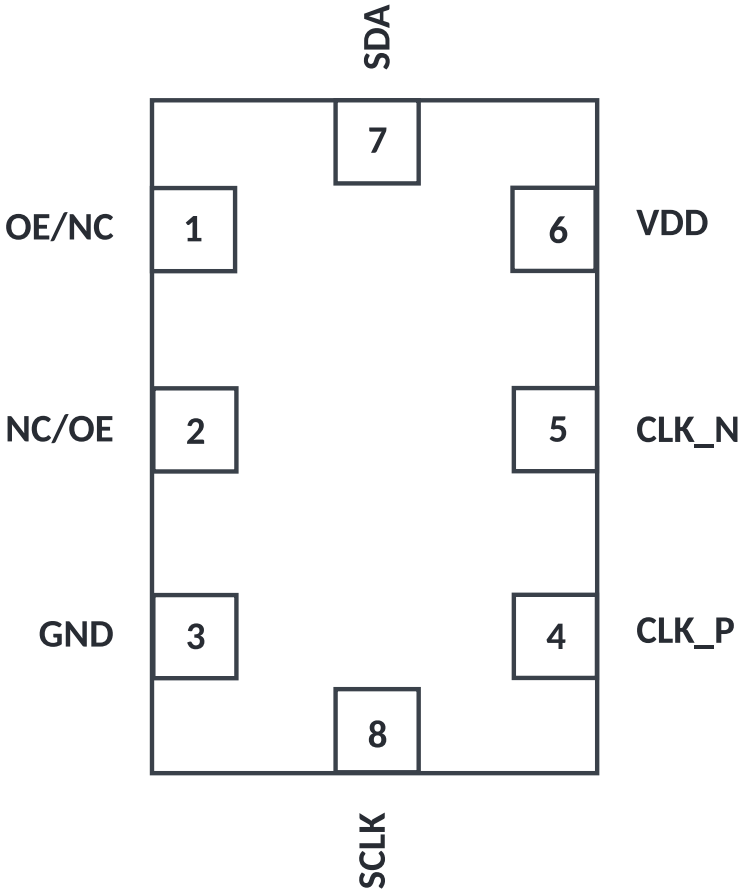


Figure 2 AU526x Top View

Table 1 Pin Description

Pin Name	I/O Type	Pin No.	Function
OE/NC	Input	1, 2	Selectable by Ordering Information OE = Output Enable; NC = No connect
GND		3	GND
CLKP	Output	4	Clock + for differential Output. Single Ended CMOS Output
CLKN	Output	5	Clock - for differential Output. Single Ended CMOS Output
VDD	Power	6	Chip Power Supply
SDA	Input/Output	7	I2C Serial Data
SCLK	Input	8	I2C Serial Clock

Notes:
The Output Enable Pin can be confgured as Active High or Low based on the customer requirement. Refer to the Ordering Information section for more details.

2 Electrical Characteristics

Table 2 Absolute Maximum Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Core supply voltage		V_{DD}	-0.5		+3.63	V
Input voltage, All Inputs	Relative to GND	V_{IN}	-0.5		+3.63	V
Storage temperature	Non-functional, Non-Condensing	T_S	-55		+150	°C
Programming Temperature		T_{PROG}	+15		+50	°C
Programming Voltage		V_{PROG}	2.375	2.5	2.625	V
ESD (human body model)	JEDEC JS-001-2012	ESD_{HBM}			2000	V
ESD (charged device model)	JEDEC JESD22-C101E	ESD_{CDM}			500	V

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 3 Operating Temperature

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Ambient temperature		TA	–40	–	+105	°C
Junction temperature		TJ			+125	°C

Table 4 DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Typ	Max	Units
Supply Voltage	1.8 V range: ±5%	V_{DD}	1.71	1.80	1.89	V
	2.5 V range: ±5%		2.375	2.50	2.625	V
	3.3 V range: ±10%		2.97	3.3	3.63	V
Supply Current (Output Enabled)	LVPECL	I_{DD}		68		mA
	LVDS			47		
	LVDS-Boost			51		
	HCSL (Far End Termination)			59		
	HCSL-LP			50		
Ambient Temperature		T_{AMB}			105	°C
Output Enable		V_{IH}	0.7x VDD			V
		V_{IL}			0.3xVDD	V
	Output Disable Time, FCLK > 10 MHz	T_D		1us+ 3clock cycles		uS
	Output Enable Time, FCLK > 10 MHz	T_E		1us+ 3clock cycles		uS
Power Up Time				15		ms

Table 5 Output RMS Jitter [AU5260]

Parameter	Conditions	Symbol	Min	Typ	Max	Units
RMS Jitter for 12 kHz – 20 MHz Integration Bandwidth	F_{OUT} = 622.08 MHz	RMS_{JIT}		110		fs rms
	F_{OUT} = 156.25 MHz					

Notes:

1. The RMS Jitter data is based on the simulation results. Final data will be populated based on lab Characterization.

Table 6 Output RMS Jitter [AU5265]

Parameter	Conditions	Symbol	Min	Typ	Max	Units
RMS Jitter for 12 kHz – 20 MHz Integration Bandwidth	F_{OUT} = 622.08 MHz	RMS_{JIT}		85		fs rms
	F_{OUT} = 156.25 MHz					

Notes:
1. The RMS Jitter data is based on the simulation results. Final data will be populated based on lab Characterization.

Table 7 Clock Output Phase Noise [AU5260]

Offset Frequency	156.25 MHz LVDS	622.08 MHz LVDS	Units
1 kHz	-118.5	-106.5	dBc/Hz
10 kHz	-128.8	-116.8	
100 kHz	-139.5	-127.5	
1 MHz	-152.2	-140.2	
10 MHz	-167.2	-157.5	
20 MHz	-170.5	-162.7	
Offset Frequency	**156.25MHz LVPECL**	**622.08 MHz LVPECL**	**Units**
1 kHz	-118.5	-106.5	dBc/Hz
10 kHz	-128.8	-116.8	
100 kHz	-139.5	-127.5	
1 MHz	-152.2	-140.2	
10 MHz	-165.7	-157.4	
20 MHz	-169.8	-162.6	

Notes:
1. The Clock Output Phase Noise data is based on the simulation. Final Phase Noise data will be populated based on lab Characterization.

Table 8 Clock Output Phase Noise [AU5265]

Offset Frequency	156.25 MHz LVDS	622.08 MHz LVDS	Units
1 kHz	-120.7	-108.7	dBc/Hz
10 kHz	-132.7	-120.7	
100 kHz	-143.6	-131.6	
1 MHz	-151.8	-139.8	
10 MHz	-167.9	-159.1	
20 MHz	-170.6	-162.9	
Offset Frequency	**156.25MHz LVPECL**	**622.08 MHz LVPECL**	**Units**
1 kHz	-120.7	-108.7	dBc/Hz
10 kHz	-132.6	-120.7	
100 kHz	-143.6	-131.6	
1 MHz	-151.7	-139.8	
10 MHz	-166.3	-158.8	
20 MHz	-169.8	-162.9	

Notes:
1. The Clock Output Phase Noise data is based on the simulation. Final Phase Noise data will be populated based on lab Characterization.

Table 9 Power Supply Rejection

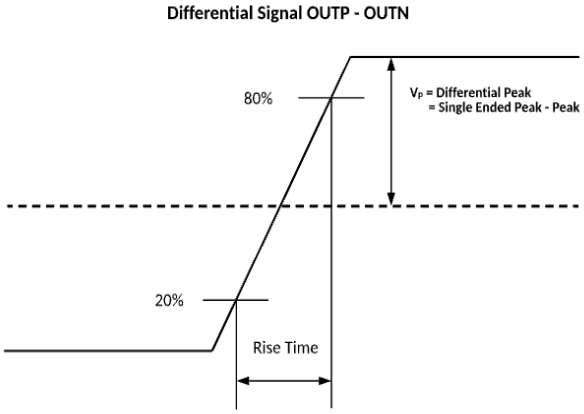
Parameter	Conditions	Symbol	Min	Typ	Max	Units
F_{OUT} = 156.25 MHz	100 kHz Sine Wave	$PSRR_{VDD}$		-85		dBc
	200 kHz Sine Wave					
	500 kHz Sine Wave					
	1 MHz Sine Wave					

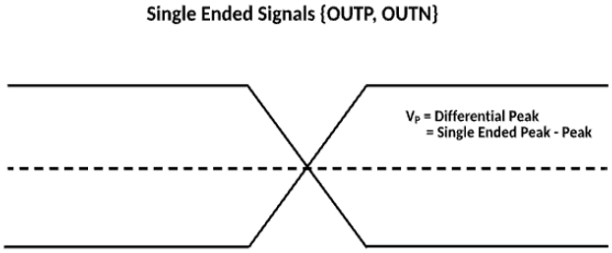
Notes:
1. The PSRR is measured with a 50 mVpp sinusoid in series with the supply and checking the spurious level relative to the carrier on the output in terms of phase disturbance impact.
2. Output PSRR measured with LVDS standard which are the recommended standards for AC Coupled terminations.
3. The PSRR data is provided based on simulation worst case numbers.Final data will be provided based on lab characterization.

Table 10 Output Clock Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
DC Electrical Specifications – LVDS Outputs (VDD = 1.8 V, 2.5 V or 3.3 V range)						
Output Common-Mode Voltage	VDD = 2.5 V or 3.3 V range	V_{OCM}		1.2		V
Output Common-Mode Voltage	VDD = 1.8 V	V_{OCM}		0.85		
AC Electrical Specifications (LVPECL, LVDS, HCSL Far End Termination): Fout = 156.25 MHz						
Clock Output Frequency		f_{OUT}	0.2		1000	MHz
LVPECL Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVPECL outputs.	t_{RF}			350	ps
LVDS Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	t_{RF}			350	ps
LVDS-Boost Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for LVDS outputs.	t_{RF}			350	ps
HCSL Far End Termination Output Rise/Fall Time	20% to 80% of AC levels. Measured at 156.25 MHz for HCSL outputs.	t_{RF}			350	ps
Output Duty Cycle	Measured at differential 50% level, 156.25 MHz	t_{ODC}	45	50	55	%
LVPECL Output Differential peak	Measured at 156.25M Output	VP		750		mV
LVDS Output differential peak	Measured at 156.25M Output	VP		400		
LVDS-Boost Output differential peak	Measured at 156.25M Output	VP		790		
HCSL Far End Termination Output differential peak	Measured at 156.25M Output	VP		800		
AC Electrical Specifications (HCSL – LP)						
Slew Rate	Scope Averaging on	dV/dt	1		4	V/ns
Slew Rate Matching	Single-ended measurement.	ΔdV/dt			20	%
Maximum Voltage	Measurement on single ended signal using absolute value. (Scope averaging off).	V_{MAX}		850		mV
Minimum Voltage		V_{MIN}		0		mV
Crossing Voltage (abs)	Scope averaging off.	V_{cross_abs}		430		mV
Crossing Voltage (var)	Scope averaging off.	Δ-V_{cross}		9.6		mV
Differential Impedance		Z_{DIFF}		85/100		Ω

Notes:
Convention for Wave Forms





3 Serial Programming Interface Description

The chip settings can be reconfigured using the I2C serial programming interface.

3.1 I2C protocol

Pin configuration of serial interface in I2C slave mode is as follows.

- SCL
- SDA

The device uses the SDA and SCL pins for a 2-wire serial interface that operates up to 400 Kb/s in Read and Write modes. It complies with the I2C bus standard. The I2C access protocol in device is both random and sequential access for Write and Read modes.

The I2C serial interface can operate at either Standard rate (100 Kbps) or Fast rate (400 Kbps).

The default I2C address will be 0x55, The Device will support to configure any I2C address through One Time Programming.

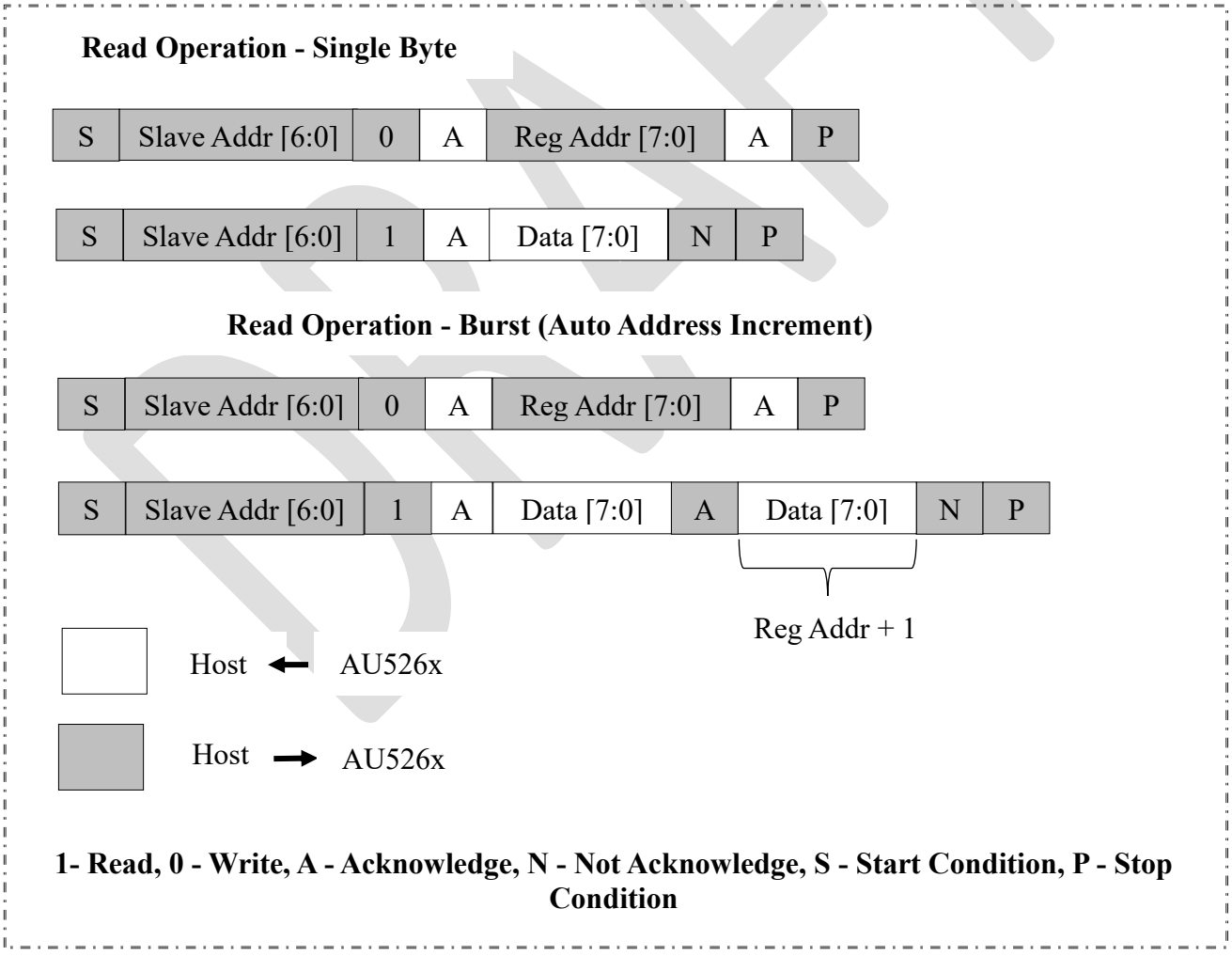


Figure 3 I2C Read Operation

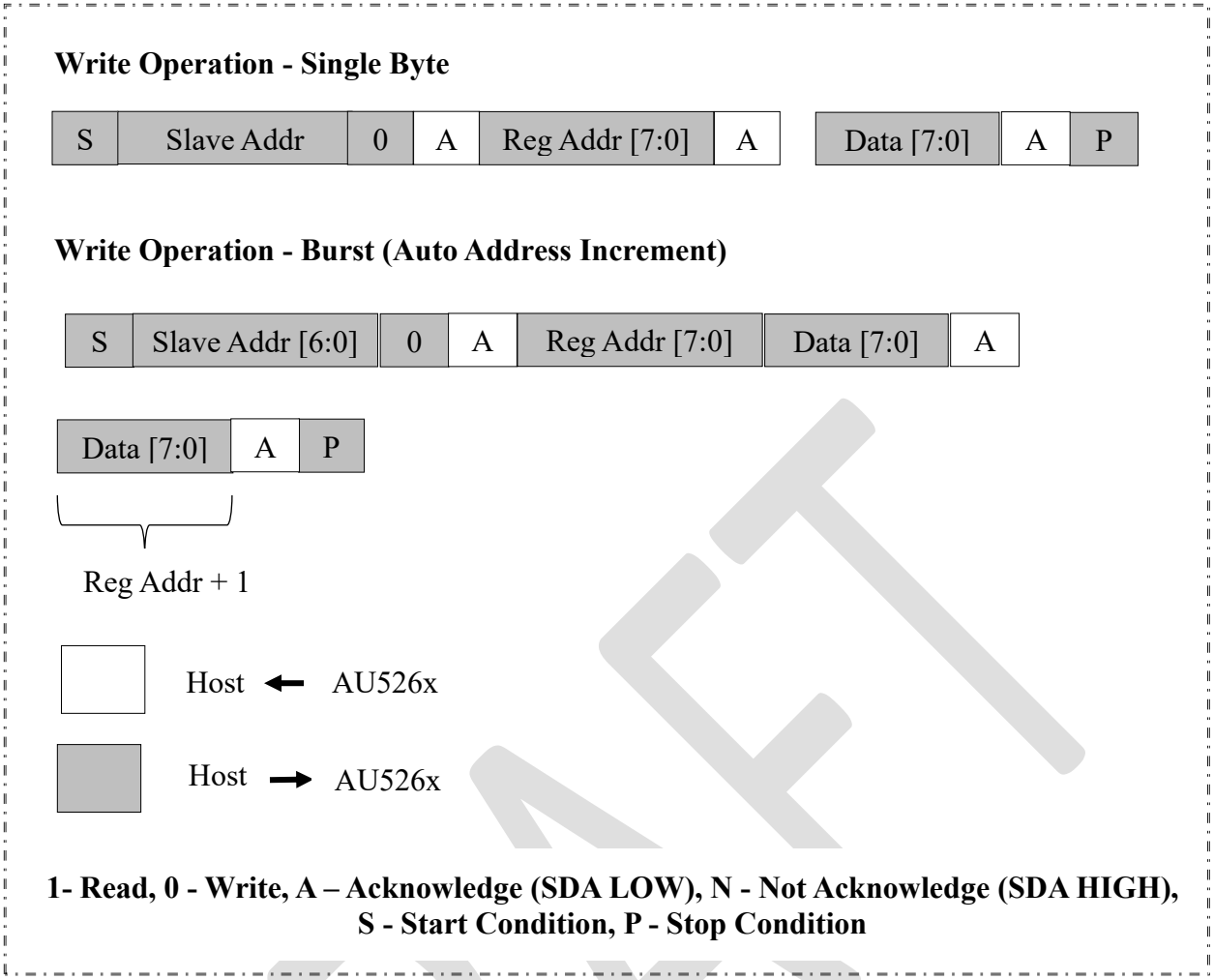


Figure 4 I2C Write Operation

3.1.1 Single Byte Write

- The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit register map address
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit data to be written to the register map address specified
- The slave acknowledges by driving zero on the bus
- The master ends the transaction by issuing a stop condition

3.1.2 Multi Byte Write

- The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit register map address
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit data to be written to the register map address specified
- The slave acknowledges by driving zero on the bus and increment the address by 1
- The master continuously writes the 8-bit data to the slave and the slave will acknowledge by driving zero for every byte.
- The master ends the transaction by issuing a stop condition

3.1.3 Single Byte Read

- The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit register map address
- The slave acknowledges by driving zero on the bus
- The master ends the transaction by issuing a stop condition
- The master re-initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 1 (read)
- The slave then writes the 8-bit data to be written to the register map address specified
- The master does not acknowledge this transaction as the slave may assume a multi-byte read operation and there is a risk of slave holding the bus low
- The master ends the transaction by issuing a stop condition

3.1.4 Multi Byte Read

The multi-byte read mode is used to read a continuous segment of the register map. The multi-byte read is faster than performing multiple single byte reads as the device address and register map address need not be specified for every byte read from the register map

- The master initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 0 (write)
- The slave acknowledges by driving zero on the bus
- The master then writes the 8-bit register map address
- The slave acknowledges by driving zero on the bus
- The master ends the transaction by issuing a stop condition
- The master re-initiates the transaction by issuing a start condition, writes 7-bit slave address and then the read/write bit is written as 1 (read)
- The slave then writes the 8-bit data to be written to the register map address specified
- The master acknowledges by driving zero on the bus
- The slave automatically increments the register map address and writes the data in at that address to the bus and the master acknowledges
- When all bytes of data are read, master ends the operation by not acknowledging the last read
- The master then ends the transaction by issuing a stop condition

3.1.5 I2C Bus Timing Specifications

Table 11 I2C Bus Timing Specification

Description	Symbol	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
SCLK clock frequency	f_{SCL}	–	100	–	400	kHz
Hold time START condition	$t_{HD:STA}$	0.4	–	0.6	–	µs
Low period of the SCK clock	t_{LOW}	4.7	–	1.3	–	µs
High period of the SCK clock	t_{HIGH}	4.0	–	0.6	–	µs
Setup time for a repeated START condition	$t_{SU:STA}$	4.7	–	0.6	–	µs
Data hold time	$t_{HD:DAT}$	300	–	300	–	ns
Data setup time	$t_{SU:DAT}$	100	–	–	–	ns
Rise time	t_R	–	1000	–	300	ns
Fall time	t_F	–	300	–	300	ns
Setup time for STOP condition	$t_{SU:STO}$	4.0	–	0.6	–	µs
Bus-free time between STOP and START conditions	t_{BUF}	4.7	–	1.3	–	µs
Data valid time	$t_{VD;DAT}$	–	3.45	–	0.9	µs
Data valid acknowledge time	$t_{VD;ACK}$	–	0.9	–	0.9	µs

Note:

- In I2C mode, the serial data and clock have an on-chip 25 kΩ pull up resistor to VDDIO. Please refer Figure 5 for the nomenclature of these parameters.

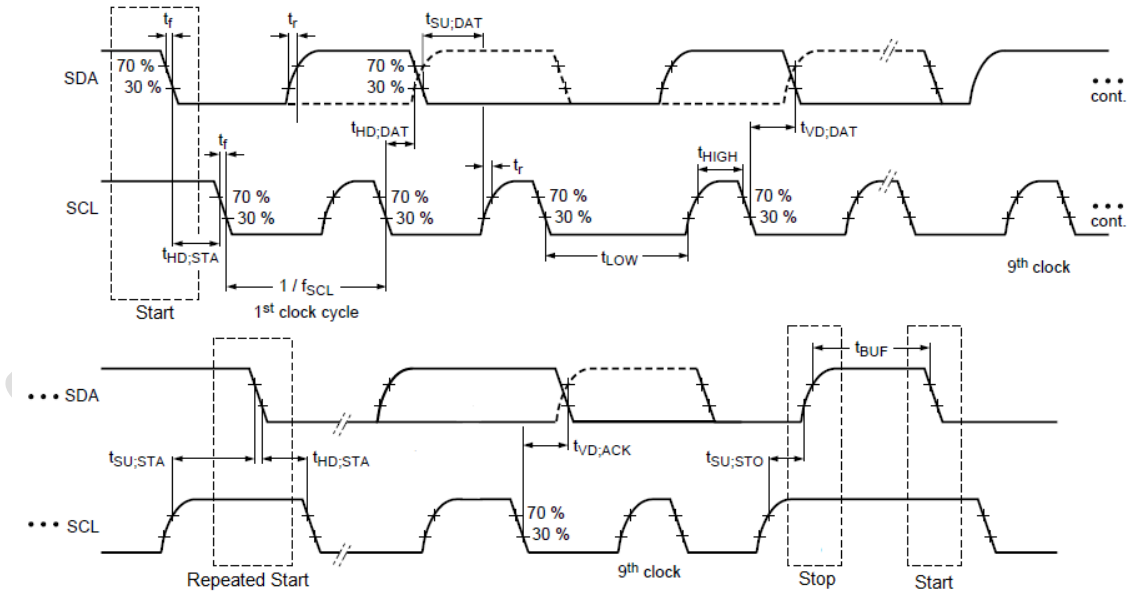


Figure 5 I2C Timing Waveform

4 Package Information

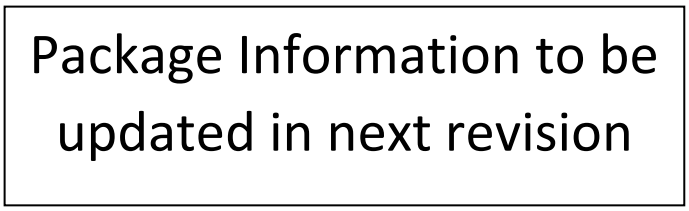


Figure 6 Package Diagram (3.2 mm x 2.5 mm)

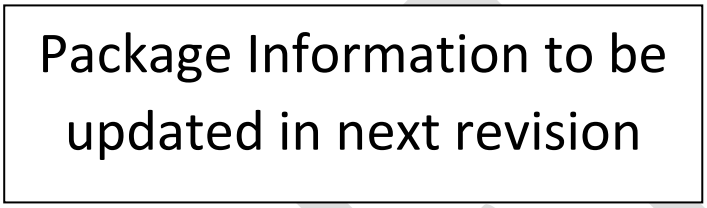


Figure 7 Package Diagram (5.0 mm x 3.2 mm)

5 Output Termination Information

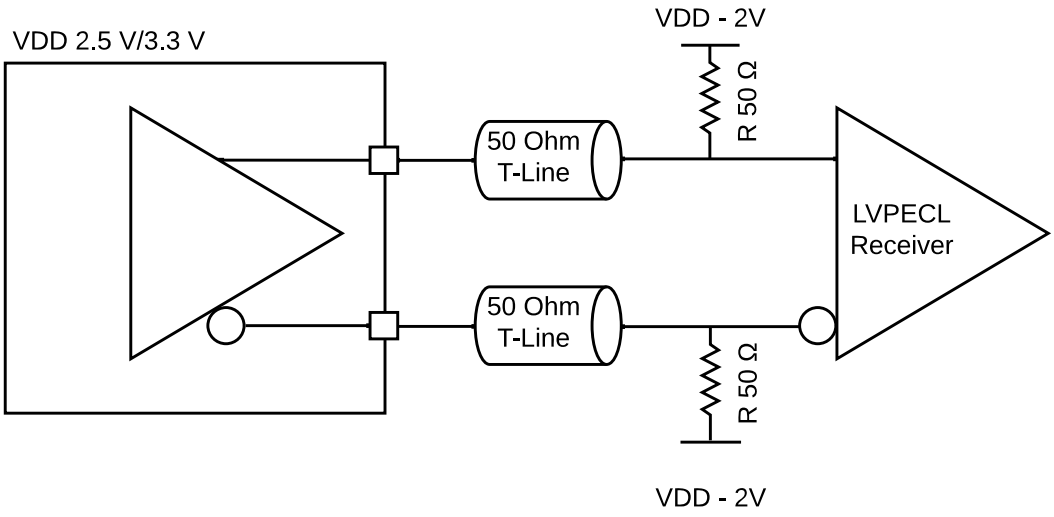
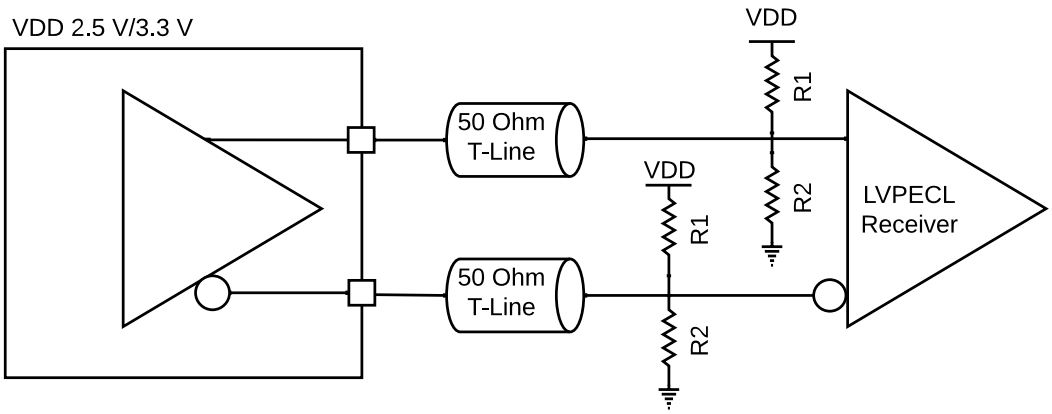


Figure 8 LVPECL Output Driver used with traditional DC Coupled LVPECL receiver



VDD	R1	R2
2.5 V	250 Ω	62.5 Ω
3.3 V	127 Ω	82.5 Ω

Figure 9 LVPECL Output Driver with DC Coupled LVPECL receiver: Thevenin Equivalent

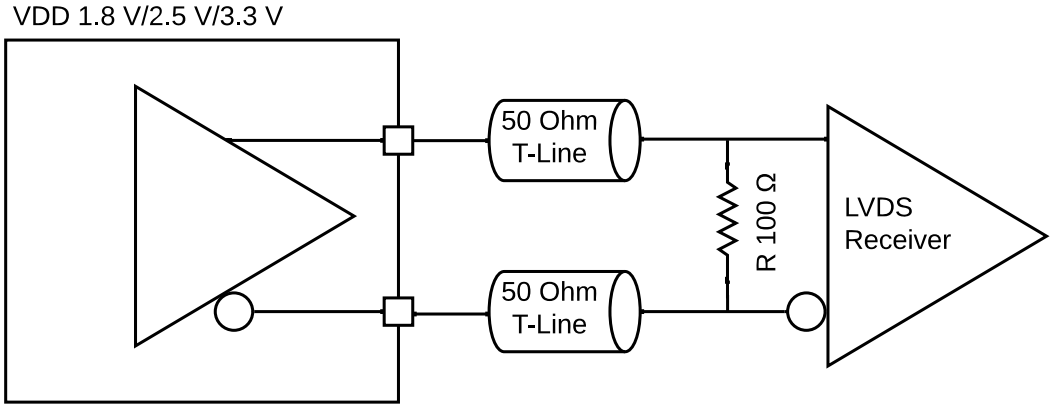


Figure 10 LVDS Output Driver used with traditional DC Coupled LVDS receiver

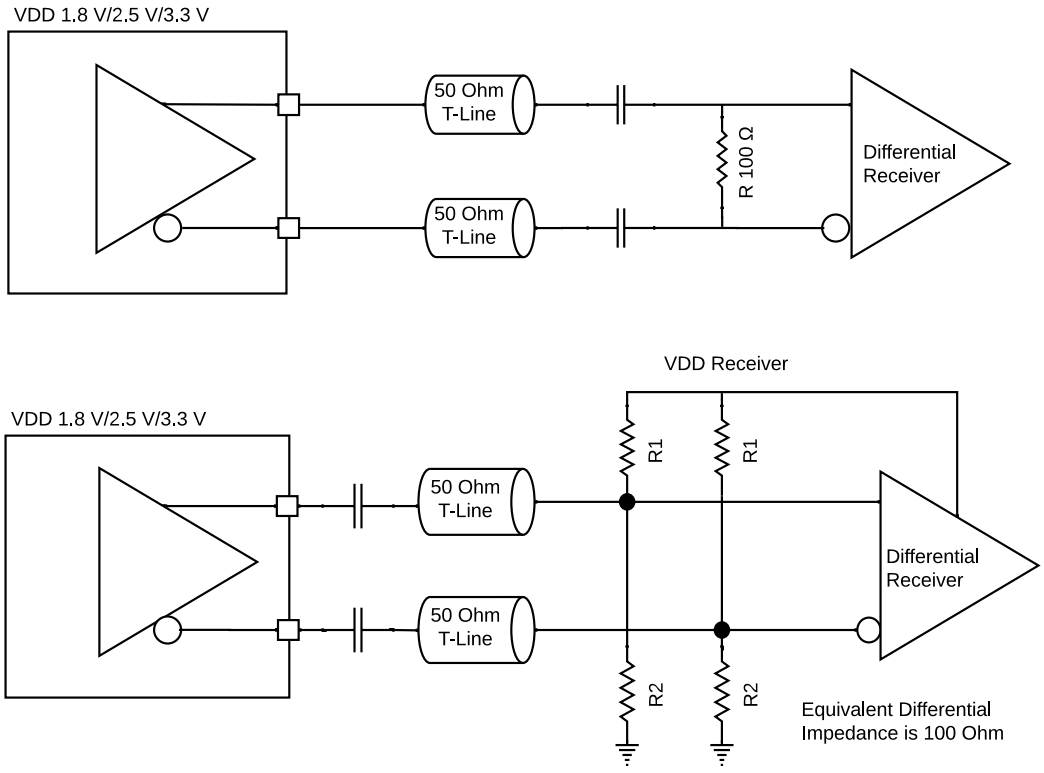


Figure 11 LVDS Output Driver used with AC Coupled terminations for various receivers

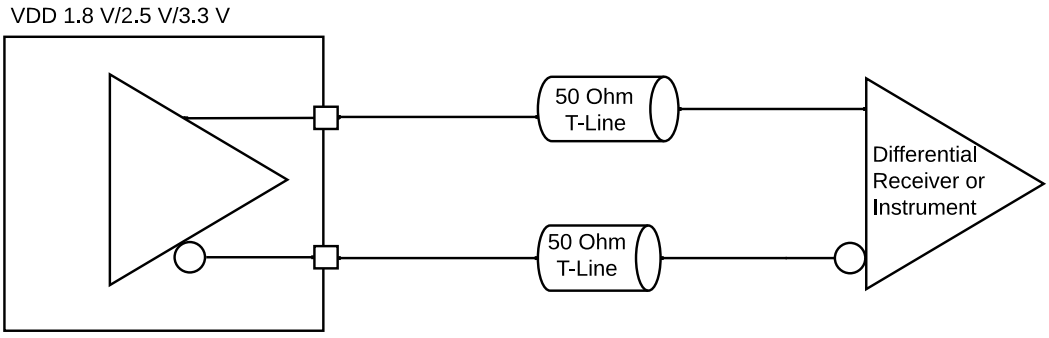


Figure 12 HCSL DC Coupled – Low-Power (HCSL-LP)

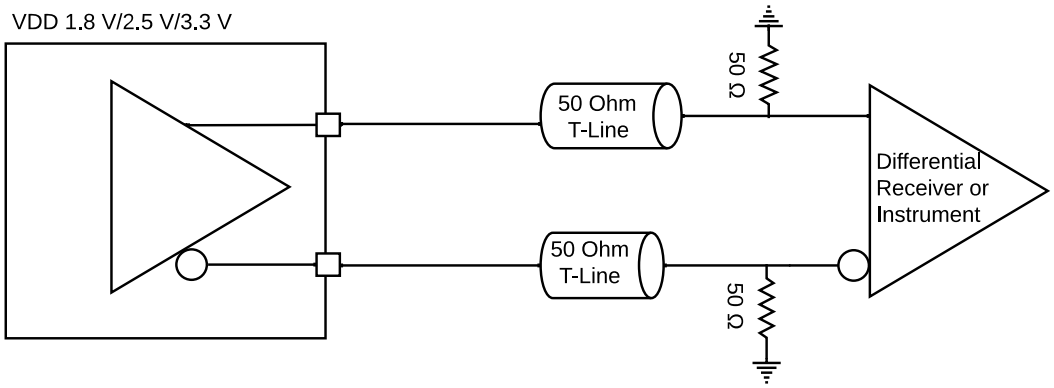


Figure 13 HCSL DC Coupled - Far End Termination

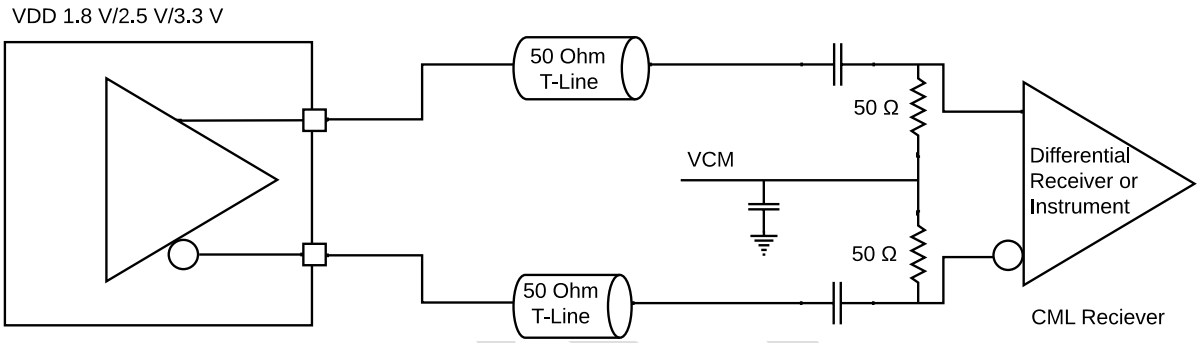


Figure 14 Output Driver with AC Coupled CML receiver

6 Ordering Information

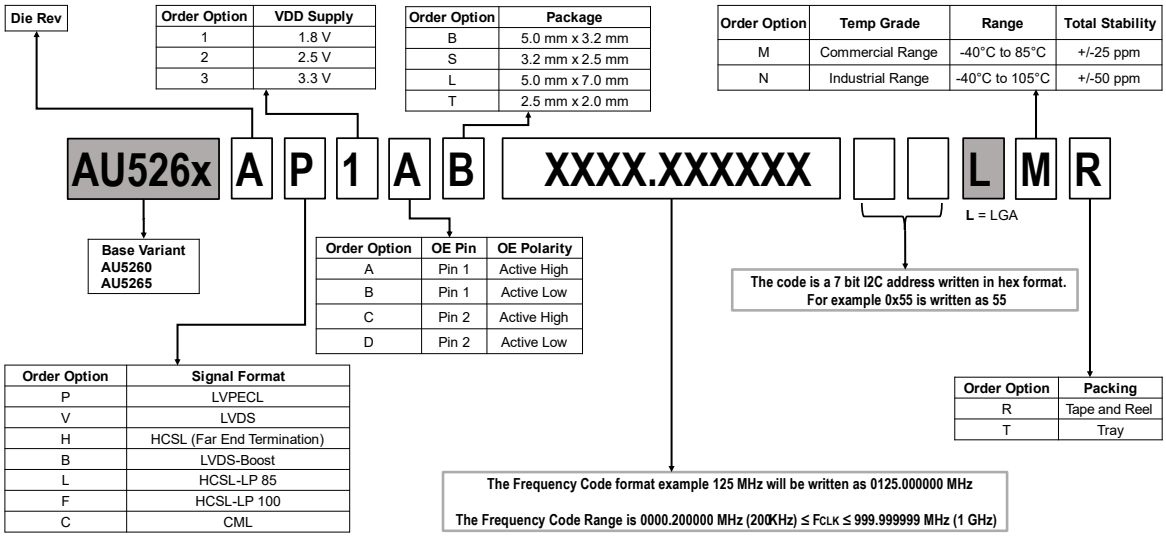


Figure 15 Ordering Information

Note: Please contact Aurasemi sales for 5.0 mm x 7.0 mm and 2.5 mm x 2.0 mm packages.

7 Revision History

Table 12 Revision History

Version	Date	Description	Author
0.1	26th Sep 2022	AU526x Advanced Datasheet First Draft Created	Aurasemi

IMPORTANT NOTICE AND DISCLAIMER

AURASEMI PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Aurasemi products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Aurasemi grants you permission to use these resources only for development of an application that uses Aurasemi products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Aurasemi intellectual property or to any third-party intellectual property. Aurasemi disclaims responsibility for, and you will fully indemnify Aurasemi and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Aurasemi products are provided only subject to Aurasemi Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Aurasemi resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

Contact Information

For more information visit www.aurasemi.com

For sales related information please send an email to sales@aurasemi.com

Trademarks