AU5411 – 10 OUTPUT, DIFFERENTIAL, ULTRA LOW JITTER BUFFER

General Description

The AU5411 is a 2.1 GHz, 10 output low-jitter clock fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution and level translation.

The buffer can choose a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock can be distributed to two output drive banks A, B and one LVCMOS output.

The crystal input can support crystals from 8 MHz to 50 MHz. It can also support single ended clock.

The output drivers of each bank can be independently programmed to LVPECL, LVDS, HCSL or HIZ mode. The LVCMOS clock output is synchronized to selected clock and can be enabled or disabled in a glitch free manner.

The AU5411 operates from a 3.3 V/2.5 V core supply and 3 independent 3.3 V/2.5 V output supplies. LVCMOS output driver can be operated at 1.8 V

Features

- Additive jitter performance of 55 fs RMS.
- 3:1 input clock selection
- Two universal clock inputs can operate up to 2.1 GHz and accept LVPECL, LVDS, LVCMOS, CML(ac-coupled only), HCSL, SSTL or single ended clocks
- One crystal input which can support crystals in the frequency range of 8 MHz to 50 MHz or it can accept single ended input clock.
- Two output driver banks A and B which can be programmed independently to LVPECL, LVDS, HCSL or HIZ mode.
- Typical output skew between clock outputs is 30 ps
- Level translation with core supply voltage of 3.3 V/2.5 V and 3.3 V/2.5 V output supply for differential output drivers.
- 3.3 V/2.5 V/1.8 V operation for the single LVCMOS output driver
- The AU5411 buffer is pin controlled.
- High PSRR -70/-73 dBc for LVPECL/LVDS modes
- AU5411 buffer is available in a 48-pin,
- 7mm x 7mm WQFN package.

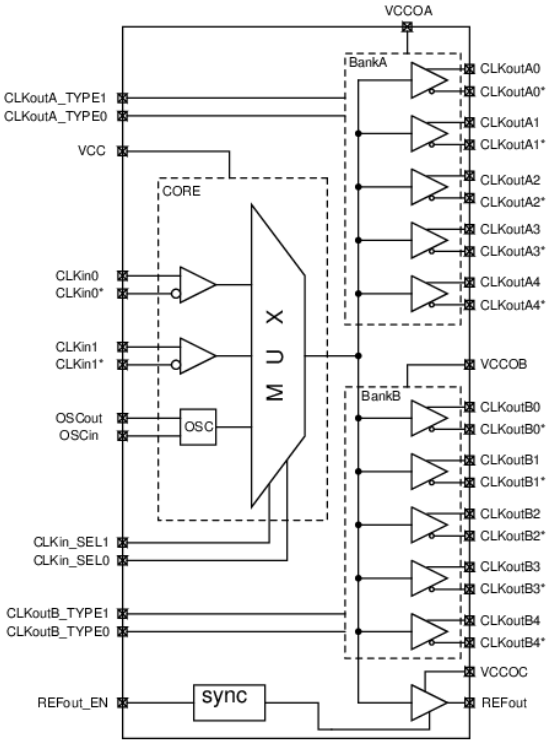

Figure 1 Functional Overview

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1 Detailed Pin Description

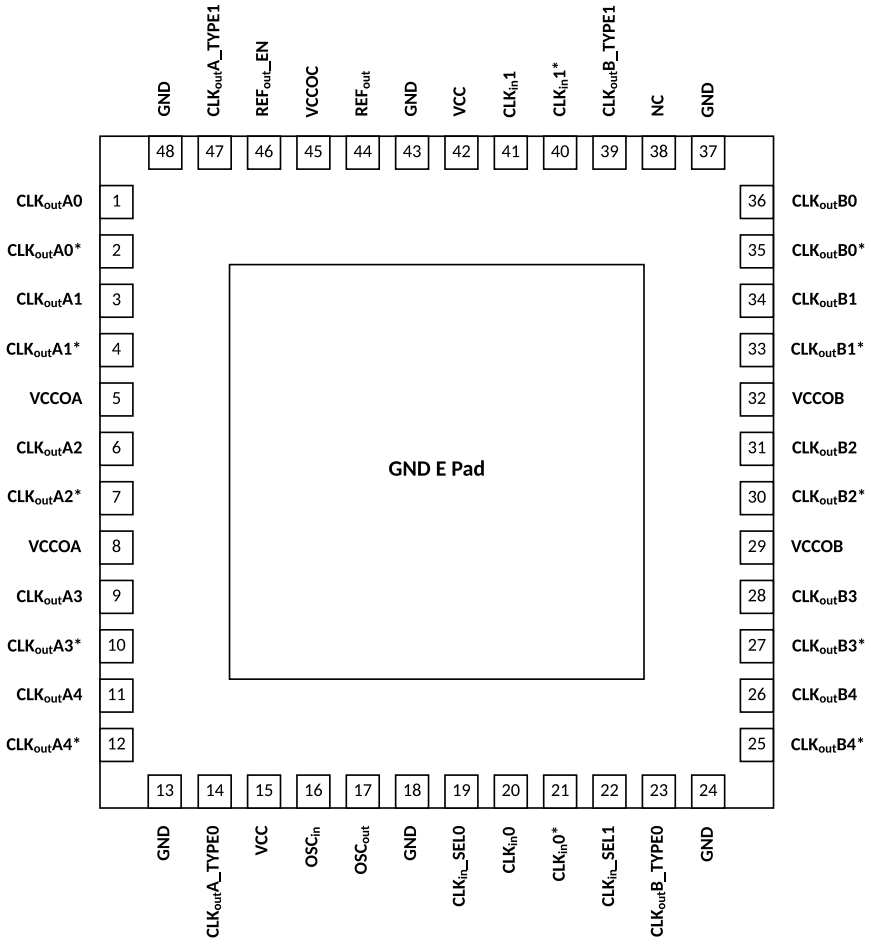


Figure 2 AU5411 Buffer, Differential Output Buffer Top View

Table 1 Detailed Pin Description

Pin Name	Pin Number	Functionality AU5411
Pin group: Bank A clock output pads		
CLKoutA0	1	Differential clock output P of A0. Output type set by CLKoutA_TYPE pins.
CLKoutA0*	2	Differential clock output N of A0. Output type set by CLKoutA_TYPE pins.
CLKoutA1	3	Differential clock output P of A1. Output type set by CLKoutA_TYPE pins.
CLKoutA1*	4	Differential clock output N of A1. Output type set by CLKoutA_TYPE pins.
CLKoutA2	6	Differential clock output P of A2. Output type set by CLKoutA_TYPE pins.
CLKoutA2*	7	Differential clock output N of A2. Output type set by CLKoutA_TYPE pins.
CLKoutA3	9	Differential clock output P of A3. Output type set by CLKoutA_TYPE pins.
CLKoutA3*	10	Differential clock output N of A3. Output type set by CLKoutA_TYPE pins.
CLKoutA4	11	Differential clock output P of A4. Output type set by CLKoutA_TYPE pins.
CLKoutA4*	12	Differential clock output N of A4. Output type set by CLKoutA_TYPE pins.
Pin group: Bank B clock output pads		
CLKoutB0	36	Differential clock output P of B0. Output type set by CLKoutB_TYPE pins.
CLKoutB0*	35	Differential clock output N of B0. Output type set by CLKoutB_TYPE pins.
CLKoutB1	34	Differential clock output P of B1. Output type set by CLKoutB_TYPE pins.
CLKoutB1*	33	Differential clock output N of B1. Output type set by CLKoutB_TYPE pins.
CLKoutB2	31	Differential clock output P of B2. Output type set by CLKoutB_TYPE pins.
CLKoutB2*	30	Differential clock output N of B2. Output type set by CLKoutB_TYPE pins.
CLKoutB3	28	Differential clock output P of B3. Output type set by CLKoutB_TYPE pins.
CLKoutB3*	27	Differential clock output N of B3. Output type set by CLKoutB_TYPE pins.

Pin Name	Pin Number	Functionality AU5411
CLKoutB4	26	Differential clock output P of B4. Output type set by CLKoutB_TYPE pins.
CLKoutB4*	25	Differential clock output N of B4. Output type set by CLKoutB_TYPE pins.
Pin group: Bank C clock output pad		
REFout	44	LVCMOS clock out synchronized with differential clocks
Pin group: Clock inputs		
CLKin0	20	Universal clock input 0 (+ve polarity) (differential/single-ended)
CLKin0*	21	Universal clock input 0 (-ve polarity) (differential/single-ended)
CLKin1	41	Universal clock input 1 (+ve polarity) (differential/single-ended)
CLKin1*	40	Universal clock input 1 (-ve polarity) (differential/single-ended)
OSCin	16	Input for crystal. It can be over driven by an AC coupled single ended clock in crystal over drive mode. In the external bypass mode, the max voltage at the pin needs to be 1.5V. If the dirver is swinging to say 3.3V rail, then a resistor divider is needed on PCB to restrict the swing at Oscin to 1.5V Cload supported 6pF to 10pF, freq 8MHz to 50 MHz
OSCout	17	Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.
Pin group: Power pins		
VCC	15	Line supply - 3.3V/2.5V
VCC	42	Line supply - 3.3V/2.5V
VCCOA	5	Power supply for Bank A Output buffers. VCCOA can operate from 3.3 V or 2.5 V. 1.8V is supported for HCSL driver.
VCCOA	8	Power supply for Bank A Output buffers. VCCOA can operate from 3.3 V or 2.5 V. 1.8V is supported for HCSL driver.
VCCOB	32	Power supply for Bank B Output buffers. VCCOB can operate from 3.3 V or 2.5 V. 1.8V is supported for HCSL driver.
VCCOB	29	Power supply for Bank B Output buffers. VCCOB can operate from 3.3 V or 2.5 V. 1.8V is supported for HCSL driver.
VCCOC	45	Power supply for Bank C Output buffer. VCCOC can operate from 3.3 V or 2.5 V or 1.8 V
GND-EPAD	0	Ground
GND	13	ground pin
GND	18	ground pin
GND	24	ground pin
GND	37	ground pin
GND	48	ground pin
GND	43	ground pin
Pin group: Control pins		
CLKoutA_Type0	14	Bank A output buffer type selection pins
CLKoutA_Type1	47	Bank A output buffer type selection pins
CLKoutB_Type0	23	Bank B output buffer type selection pins
CLKoutB_Type1	39	Bank B output buffer type selection pins
REFout_EN	46	REFout enable input. Enable signal is internally synchronized to selected clock input.
CLKin_SEL0	19	Clock input selection pins
CLKin_SEL1	22	Clock input selection pins
NC	38	No Connect, It should never be pulled high. It can be pulled low or left floating. If pulled high, chip behavior will not be determined and is probabilistic.

2 Electrical Characteristics

Table 2 Absolute Maximum Ratings

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Core supply voltage, Analog Input		V_{CC}	-0.3		3.6	V
Output bank supply voltage		V_{CCO}	-0.3		3.6	V
Input voltage, All Inputs, except XIN		V_{IN}	-0.3		3.6	V
XIN		V_{IN}	-0.3		1.5	V
Storage temperature		TS	-55		150	°C

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 3 Recommended Operating Supply and Temperatures

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Core supply voltage		VCC	3.135	3.3	3.45	V
		VCC	2.375	2.5	2.625	V
Output supply voltage		VCCOA/B	3.135	3.3	3.45	V
		VCCOA/B	2.375	2.5	2.625	V
		VCCOA/B (Only for HCSL)	1.71	1.8	1.89	V
Output supply voltage for LVCMOS driver		VCCOC	3.135	3.3	3.45	V
Output supply voltage		VCCOC	2.375	2.5	2.625	V
Output supply voltage		VCCOC	1.71	1.8	1.89	V
Ambient Temperature		TA	-40		85	°C
Junction Temperature		TJ			125	°C

Table 4 Electrical Characteristics

Unless otherwise specified: Vcc = 3.3 V ± 5%, 2.5 V ± 5%,Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, TA = 25 °C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Current Consumption						
Core supply current when input buffer is selected	CLKIN0/1 selected, V_{CC} = 3.3 V/2.5 V ± 5%, V_{CC} = V_{CCO}	I_{CC_CORE}		16.5	19.8	mA
Core supply current when Crystal is selected	XO selected, V_{CC} = 3.3 V/2.5 V ± 5%, V_{CC} = V_{CCO}	I_{CORE_XO}(4)			14	mA
Increment in core supply when all ODR banks are enabled		$I_{CC\_ODR\_EN}$			2	mA
Frequency dependent current both bank on core supply. This current scales with frequency	For F_{in} = 2100 MHz	I_{CC_DYN}(1)(4)		25	33	mA
Additive output supply current per LVPECL bank enabled		I_{CCO_PECL}		165	204	mA

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive output supply current per LVDS bank enabled		I_{CCO_LVDS}		40	49	mA
Additive output supply current per HCSL bank enabled		I_{CCO_HCSL}		110	138	mA
Additive output supply current, LVCMOS Output Enabled	F_{IN} = 200 MHz, C_{LOAD} = 5 pF, V_{CCO} = 3.3 V	I_{CCO_CMOS}		6	7.2	mA
	F_{IN} = 200 MHz, C_{LOAD} = 5 pF, V_{CCO} = 2.5 V			4.5	5.5	mA
Power Supply Rejection Ratio						
Ripple induced phase spur level, supply ripple of 100mV pp	Fin = 156.25 MHz, Foffset = 100 KHz VCCOA/B = 2.5 V	$PSRR_{PECL}$		-67		dBc
Ripple induced phase spur level, supply ripple of 100mV pp	Fin = 156.25 MHz, Foffset = 100 KHz VCCOA/B=2.5 V	$PSRR_{LVDS}$		-70		dBc
Ripple induced phase spur level, supply ripple of 100mV pp	Fin = 156.25 MHz, Foffset = 100 KHz VCCOA/B = 2.5 V	$PSRR_{HCSL}$		-67.7		dBc
Input High Current	V_{CC} = 3.3V, V_{IH} = V_{CC}	I_{IH}		30	50	µA
Input Control Pin Characteristic						
Input Low Current		I_{IL}	-20	0.1		µA
Input high voltage – Logic inputs		V_{IH}	0.7*VCC		VCC	V
Input low voltage – Logic inputs		V_{IL}	GND		0.3*VCC	V
Internal Pull-down resistance		$R_{pulldown}$		200		K Ω

Notes:

1. Total current from core supply at frequency Fin = $I_{CORE,\ STATIC}$ + N*(0.5*Fin/2100M)* $I_{CORE,\ DYN.}$ Detailed methodology of calculating the power dissipated in each ODR mode is given in the section “Current consumption and Power Dissipation Calculations.” N is the number of output banks enabled.
2. Refer to Section 4.1 for more information on current consumption and power dissipation calculations.
3. Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the Vcco supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [(2 * 10(PSRR / 20)) / (π * f_{CLK})] * $1E^{12}$
4. Specification is ensured by characterization and is not tested in production.

Table 5 Input Clock Characteristics

Unless otherwise specified: Vcc = 3.3 V ± 5%, 2.5 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, TA = 25 °C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Characteristics of Universal Input Clock Pins						
Input frequency range(4)		F_{CLKin} (1)	DC		2100	MHz
Differential input high voltage	CLKin driven differentially	V_{IHD}			VCC	V
Differential input low voltage		V_{ILD}	GND			V

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Peak differential input voltage swing(2)		V_{ID}	0.15		1.3	V
Differential input common mode voltage	Input differential swing of 150 mV	V_{CMD}	0.25		VCC-1.2	V
	Input differential swing of 350 mV		0.25		VCC-1.1	V
	Input differential swing of 800 mV		0.25		VCC-0.9	V
Single ended input high voltage	Inverting differential input held at VCC/2, VCC = 3.3 V	V_{IH}	2		VCC	V
	Inverting differential input held at VCC/2, VCC = 2.5 V		1.6		VCC	
Single ended input low voltage	Inverting differential input held at VCC/2, VCC = 3.3 V	V_{IL}	GND		1.3	V
	Inverting differential input held at VCC/2, VCC = 2.5 V		GND		0.9	
Single ended input voltage swing (3)		V_{I_SE}	0.3		2	VPP
Single ended input common mode voltage		V_{CM}	0.25		VCC-1.2	V
Mux Isolation between the two input clock paths	Fin = 100 MHz, Foffset > 50 KHz	ISO_{MUX}(1)		-84		dBc
	Fin = 200 MHz, Foffset > 50 KHz			-82		dBc
	Fin = 500 MHz, Foffset > 50 KHz			-71		dBc
	Fin = 1000 MHz, Foffset > 50 KHz			-65		dBc
Crystal Characteristics						
Equivalent series resistance		ESR		35	60	Ω
Load capacitance		CL	6	8	10	pF
Shunt Capacitance		Co		2	3	pF
Power dissipated in the crystal		Drive level		100	200	uW
Mode of oscillation				Funda--mental		
Crystal frequency range		F_{OSC}(1)	8		50	MHz
External clock frequency range	XO over drive or Bypass mode	F_{CLK}			250	MHz
Maximum swing level on OSCin/OSCout pins	XO over drive or Bypass mode	Vmax			1.5	V
Additive jitter(3)	RMS, integration BW 12 KHz to 5 MHz, $F_{crystal}$ = 25 MHz. Crystal input select Measured at VCC = VCCO = 2.5 V	t_{jit}(1)		155		fs

Notes:

1. Specification is ensured by characterization and is not tested in production.
2. Refer to Section 7 for definition of VID and VOD voltages.
3. For clock input frequency ≥ 100 MHz, CLKinX can be driven with single-ended (LVCMOS) input swing up to 3.3 Vpp. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 Vpp max to prevent input saturation (refer to Driving the Clock Inputs for interfacing 2.5 V/3.3 V LVCMOS clock input < 100 MHz to CLKinX).
4. If the input clock is initially absent when the chip is just powered up, it will take atleast 2 falling edge of clock cycles for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edge of input clock

Table 6 Output Clock Characteristics – LVPECL

Unless otherwise specified: Vcc = 3.3 V ± 5%, 2.5 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin0/1 driven differentially, input slew rate ≥3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, TA = 25 °C. Termination is 50 Ω to VCCO -2V

Parameters	Condition	Symbol	Min	Typ	Max	Unit
LVPECL						
Maximum output frequency, full VOD swing ≥ 600 mV(1)	50 Ω termination biased with VCCO -2V	F_{CLKOUT_F}(1)	1000	1200	-	MHz
Maximum output frequency, full VOD swing ≥ 400 mV(1)			1500	2100		MHz
Additive RMS jitter(1)	Integration bandwidth from 10 KHz to 20 MHz, F_{IN} = 156.25 MHz, SR > 3 V/ns 50 Ω termination biased with VCCO -2V	$Jitter_{ADD}$(1)		55		fs(rms)
Noise floor for Foffset > 10 MHz	50 Ω termination biased with VCCO-2V, F_{IN} = 156.25 MHz, SR > 3 V/ns	$Noise_{FLOOR}$(1)		-159		dBc
Output Duty Cycle	50 Ω termination biased with VCCO -2V	ODC	45		55	%
Output high voltage	50 Ω termination biased with VCCO -2V	V_{OH}	VCCO – 1.165		VCCO – 0.75	V
Differential output voltage	50 Ω termination biased with VCCO -2V	V_{OD}	475	678	960	mV
Output low voltage	50 Ω termination biased with VCCO -2V	V_{OL}	VCCO – 2.0		VCCO – 1.45	V
Output rise time, 20% to 80%	50 Ω termination biased with VCCO -2V	t_R		210	350	ps
Output fall time 20% to 80%	50 Ω termination biased with VCCO -2V	t_F		210	350	ps
Input to output delay	50 Ω termination biased with VCCO -2V	t_{pd}		876	1100	ps

Notes:

1. Specification is guaranteed by characterization and is not tested in production

Table 7 Output Clock Characteristics - LVDS

Unless otherwise specified: Vcc = 3.3 V ± 5%, 2.5 V ± 5%, Vcco = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at Vcc = 3.3 V, Vcco = 3.3 V, TA = 25 °C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
LVDS						
Maximum output frequency, full VOD swing ≥ 250 mV	R_L = 100 Ω, differential	F_{CLKOUT_FS}(1)	1000	1600	-	MHz

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Maximum output frequency, full VOD swing ≥ 200 mV	R_L = 100 Ω, differential		1500	2100		MHz
Additive RMS jitter	Integration bandwidth from 10 KHz to 20 MHz, Fin = 156.25 MHz, SR > 3 V/ns R_L = 100 Ω, differential	$Jitter_{ADD}$		60		fs(rms)
Noise floor for Foffset > 10 MHz	Fin = 156.25 MHz, SR > 3 V/ns R_L = 100 Ω, differential	$Noise_{FLOOR}$		-159		dBc
Output Duty Cycle	R_L = 100 Ω, differential	ODC	45		55	%
Change in VPP between complementary output states	R_L = 100 Ω, differential	ΔVPP			50	mV
Output differential peak voltage	R_L = 100 Ω, differential	V_{OD}	247		454	mV
Output Common-Mode Voltage	R_L = 100 Ω, differential	V_{OCM}	1.125	1.2	1.375	V
Output rise time, 20% to 80%	R_L = 100 Ω, differential, C_L < 5 pF	t_R		210	350	ps
Output fall time 20% to 80%	Uniform transmission line up to 10 inches with characterisitic impedance of 50 Ω	t_F		210	350	ps
Input to output delay		t_{pd}		840	1100	ps
Skew between outputs	VCCO = 3.3 V, 2.5 V	T_{sk}		30		ps

Notes:

1. Specification is ensured by characterization and is not tested in production.

Table 8 Output Clock Characteristics - HCSL

Parameters	Conditions	Symbol	Min	Typ	Max	Units
HCSL						
Maximum output frequency	R_L= 50 Ω to GND	F_{CLKOUT_F}[1]	DC		700	MHz
Additive RMS jitter	Integration bandwidth from 10 KHz to 20 MHz, Fin = 156.25 MHz, SR > 3 V/ns R_L = 50 Ω to GND	$Jitter_{ADD}$(1)		55		fs(rms)
Noise floor for Foffset > 10 MHz		$Noise_{FLOOR}$(1)		-159		dBc
Output Duty Cycle		ODC	45		55	%
Output Low Voltage Min	R_L = 50 Ω to GND	V_{MIN}	-300			mV
Differential Output High Voltage		V_{OH}	600	840	1150	mV
Differential Output Low Voltage		V_{OL}	-150	28	150	mV

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Absolute Crossing point voltage	R_L = 50 Ω to GND, C_L < 5 pF	V_{CROSS}	250		550	mV
Variation of V_{CROSS} over all rising clock edges		V_{CROSS} DELTA			140	mV
Output rise time, 20% to 80%	F_{IN} = 156.25 MHz, Uniform transmission line up to 10 inches with characterisitic impedance of 50 Ω R_L = 50 Ω to GND, C_L < 5 pF	t_R		210	500	ps
Output fall time 20% to 80%		t_F		210	500	ps
Input to output delay		t_{pd}		825	1100	ps

Notes:
1. Specification is ensured by characterization and is not tested in production.

Table 9 Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architecture

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Additive Phase Jitter	PCIe Gen 1[1,2,3,4]	$tj_{phPCIeG1-CC}$		2	5	ps (p-p)
	PCIe Gen 2[1,2,3,4]	$tj_{phPCIeG2-CC}$		0.08	0.15	ps(rms)
	PCIe Gen 3[1,2,4,6]	$tj_{phPCIeG3-CC}$		0.03	0.07	ps(rms)
	PCIe Gen4[1,2,4,6]	$tj_{phPCIeG4-CC}$		0.03	0.07	ps(rms)
	PCIe Gen5[1,2,4,6]	$tj_{phPCIeG5-CC}$		0.01	0.02	ps(rms)

Notes:
1. Applies to all the differential outputs, gauranteed by design and characterization.
2. Applies to all the Outputs when driven by a low phase noise source SMA100B.
3. Additive RMS Jitter Measurements were made using DSA90804A for minimum waveform length of ≥ 100k cycles with a minimum sampling rate of ≥ 40GSa/s with the waveform covering 90% of the DSO screen. All the post processing the DSO is disabled to decrease the additonal jitter impact from oscilloscope. Broadband oscilloscope noise is also minimized in the measurement.
4. Additive jitter for RMS values is calculated by solving the equation for b [b=sqrt(c^2-a^2) where 'a' the rms input jitter and "c" is the rms total jitter.
5. Input to AU5411 is fed using low phase noise source SMA100B, AU5411 is configured as 100MHz HCSL Output Driver [VCCOx = 3.3V] and fed to the channels of DSA90804A using the exact measurement set up [Refer Note 6]
6. AU5411 PCI Express Additive RMS Jitter Measurement Set up configuration

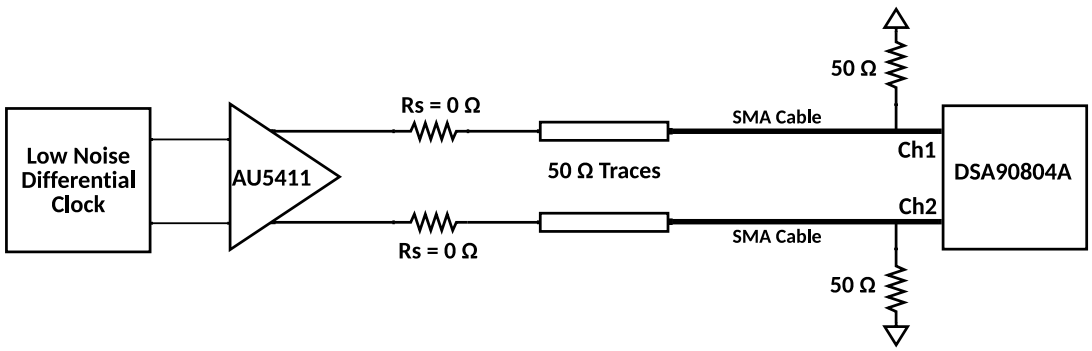


Table 10 Output Clock Characteristics – LVCMOS

Unless otherwise specified: VCC = 3.3 V ± 5%, VCCO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKin0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VCC = 3.3 V, VCCO = 3.3 V, TA = 25 °C.

Parameters	Conditions	Symbol	Min	Typ	Max	Units
Output Frequency		f_{CLKOUT}	0		250	MHz
Additive RMS jitter	VCCOC = 3.3 V ± 5%	$Jitter_{ADD}$(1)		55		fs rms
	VCCOC = 2.5 V ± 5%			63		fs rms
Noise floor for Foffset > 10 MHz VCCOC	VCCOC = 3.3 V ± 5%	$Noise_{FLOOR}$(1)		-159		dBc
	VCCOC = 2.5 V ± 5%			-157		dBc
Output Duty Cycle	For Fin ≤ 200 MHz	ODC	45		55	%
	For 200 MHz < Fin < 250 MHz		40		60	%
Output high voltage	VCCOC = 3.3 V ± 5%, 1 mA pull down current	V_{OH}	VCCOC -0.1 V			V
	VCCOC = 2.5 V ± 5%, 1 mA pull down current		VCCOC -0.1 V			V
Output low voltage	VCCOC = 3.3 V ± 5%, 1 mA pull up current	V_{OL}			0.1	V
	VCCOC = 2.5 V ± 5%, 1 mA pull up current				0.1	V
Output rise time, 20% to 80%	C_{LOAD} = 5 pF, R_{LOAD} = 50 Ω AC coupled	t_R		250	450	ps
Output fall time 20% to 80%		t_F		250	450	ps
Output enable time		t_{EN}(1)			4	cycles
Output disable time		t_{DIS}(1)			4	cycles
Input to clock edge to output clock edge delay	VCCO = 3.3 V, PCB trace of 5 inch, 5 pF capacitor	t_d(1)		1.4	2.5	ns
	VCCO = 2.5 V, PCB trace of 5 inch, 5 pF capacitor			1.5	2.7	ns

Notes:

1. Specification is ensured by characterization and is not tested in production.

3 Functional Description

The AU5411 is a 10-output differential clock fan out buffer with low additive jitter that can operate up to 2.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 5 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 48-pin WQFN package.

3.1 V_{CC} and V_{CCO} Power Supplies

The AU5411 has separate 3.3/2.5 core (V_{CC}) and 3 independent 3.3 V/2.5 V output power supplies (V_{CCOA}, V_{CCOB}). HCSL can support 1.8V power supplies (V_{CCOA}, V_{CCOB}) .V_{CCOC} supply can operate on 3.3 V/2.5 V/1.8 V rail. Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V_{OH}, V_{OL}) and LVCMOS (V_{OH}) are referenced to its respective V_{CCO} supply, while the output levels for LVDS and HCSL are relatively constant over the specified V_{CCO} range.

3.2 Clock Inputs

The input clock can be selected from CLKin0/CLKin0*, CLKin1/CLKin1*, or OSCin. Clock input selection is controlled using the CLKin_SEL[1:0] inputs as shown in Table 11. When CLKin0 or CLKin1 are selected, the oscillator is power down. The user can float OSCin and OSCout pins, since these pins are internally pulled down. OSCin is pulled down with a 56 KΩ resistance.

Table 11 Input Clock Selection

CLKin_SEL[1]	CLKin_SEL[0]	Selected Clock
0	0	CLKin0, CLKin0*
0	1	CLKin1, CLKin1*
1	0	Crystal Or Crystal Bypass AC Coupled mode
1	1	Crystal bypass DC Coupled mode

3.3 Clock States (Input vs Output States)

Table 12 Input versus Output Stages

State of Selected Clock input	Output State
Inputs are floating	Logic low
Inputs are logic low	Logic low
Inputs are logic high	Logic high

3.4 Output Driver Type

The differential output buffer type for Bank A and Bank B outputs can be separately configured using the CLKoutA_TYPE[1:0] and CLKoutB_TYPE[1:0] inputs, respectively, as shown Table 13. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, it is recommended to disable (Hi-Z) the bank to reduce power.

Table 13 OE Functionality

CLKOUTX_TYPE1	CLKOUTX_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

3.5 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the VCCOC voltage. REFout can be enabled or disabled using the enable input pin, REFout_EN, as shown in Table 14. The reference output clock is internally synchronized to the selected clock. This avoids any glitches or runt pulses while enabling or disabling the reference clock. Pulling REFout_EN to LOW, forces the outputs to the high-impedance state with in 4 falling edges of the input signal. The outputs remain in the high-impedance state as long as REFout_EN is LOW. When REFout_EN goes from HIGH to LOW, the output clock is disabled with in 4 falling edges of the input clock signal. The output is disabled at the falling edge of the input clock. This allows to disable the output clock in a glitch free manner.

When REFout_EN goes from low to high, the output clock is enabled within a time delay td, where td is given by the following equation.

$t_{d,refout\_en} = 0.5n + 3 * T_{in}$. Tin is the time period of the input clock.

When REFout_EN is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout_EN is configured with a 1K Ω load to ground, then the output will be pulled to low when disabled.

Table 14 Reference Output Enable

Refout_EN	Output State
0	Disabled (HiZ)
1	Enabled

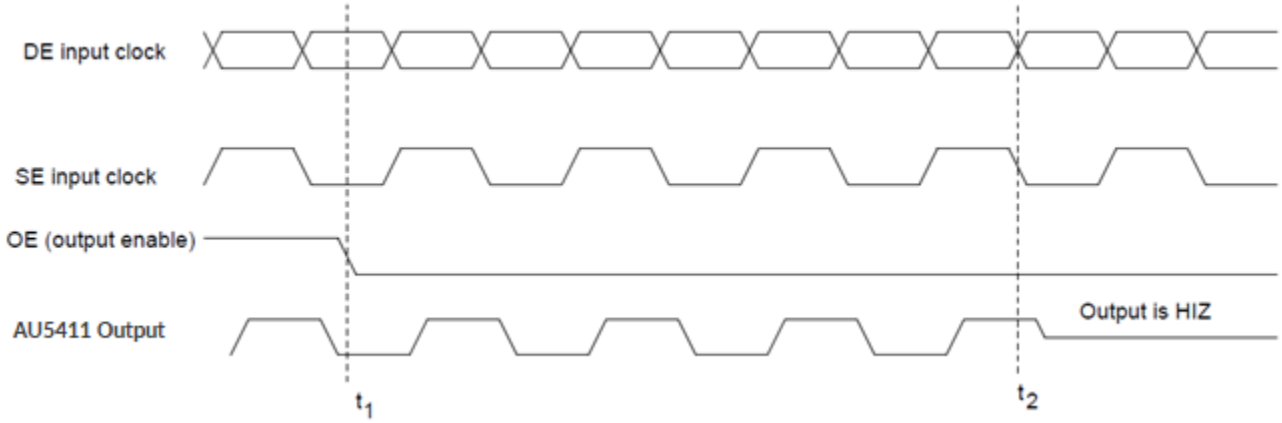


Figure 3 REFout_EN: Output disable

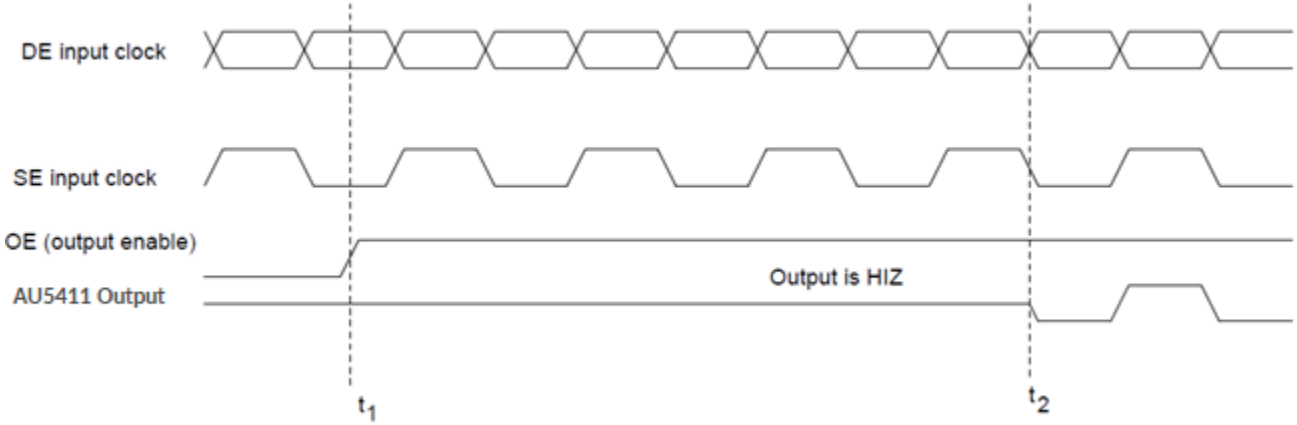


Figure 4 REFout_EN: Output enable

4 Application Information

4.1 Current consumption and Power Dissipation Calculations

The current consumption specified in the Electrical Characteristics can be used to calculate the total power dissipation and the IC power dissipation for any output driver configuration. The total current drawn from the VCC is given by the equation below.

$$I_{CC} = I_{CORE,STATIC} + n * \left(\frac{f_{in}}{100}\right) * I_{CORE,DYN}$$

I_{CC}, is the total core current drawn from VCC. $I_{CORE,STATIC}$, is the current taken by AU5411, if not clocks are toggling and both the output driver banks are in HIZ state. $I_{CORE,DYN}$, is the switching current taken from VCC when the selected input clock is toggling at a frequency of f_{in}. n, is the number of output banks that are active.

Current consumed the output supplies in each mode are listed below. The current in output bank A/B in LVPECL mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC\_LVPECL}$$

The current in output bank A/B in LVDS mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC\_LVDS}$$

The current in output bank A/B in HCSL mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC\_HCSL}$$

The current in output bank C is given below.

$$I_{CCOC} = I_{CC\_LVCMOS}$$

The equation for the total power dissipation is given below.

$$P_{TOTAL} = V_{CC} * I_{VCC} + V_{CCOA} * I_{CCOA} + V_{CCOB} * I_{CCOB} + V_{CCOC} * I_{CCOC}$$

If the output driver configuration is LVPECL or LVDS, then the power dissipated in any termination resistors and termination voltages need to be accounted to calculate the power dissipation in the device.

The power dissipated in the termination resistor in LVPECL mode is given below.

$$P_{RT\_PECL} = \frac{\left(V_{OH\_PECL} - V_{TT}\right)^2}{R_T} + \frac{\left(V_{OL\_PECL} - V_{TT}\right)^2}{R_T}$$

The power dissipated in the termination voltage for LVPECL mode is given below

$$P_{VTT\_PECL} = V_{TT} * \left(\frac{\left(V_{OH\_PECL} - V_{TT}\right)}{R_T} + \frac{\left(V_{OL\_PECL} - V_{TT}\right)}{R_T}\right)$$

The power dissipated in the ground referenced termination resistor for HCSL is given below.

$$P_{RT\_HCSL} = \frac{V_{OH\_HCSL}^2}{R_T}$$

The power dissipated in the device is given below.

$$P_{DEVICE} = P_{TOTAL} - N_1 * \left(P_{RT_{PECL}} + P_{VTT_{PECL}}\right) - N_2 * P_{RT\_HCSL}$$

4.1.1 Example: Worst case power dissipation

BANK A and B output drivers are configured in LVPECL mode. The input frequency is 2100 MHz. VCC = 3.465, VCCOA = VCCOB = VCCOC = 3.465, REFOUT is enabled. Assume 5 pF load for REFOUT.

Table 15 Worst Case Power Dissipation

Parameter	Value	Unit
V_{CC}	3.465	V
V_{CCOA}	3.465	V
V_{CCOB}	3.465	V
V_{CCOC}	3.465	V
I_{CC}	52	mA
I_{CCOA}	198	mA
I_{CCOB}	198	mA
I_{CCOC}	10	mA
P_{TOTAL}	1588	mW
V_{OH_PECL}	2.5	V
V_{OL_PECL}	1.8	V
V_{TT}	1.465	V
P_{RT_PECL}	24	mW
P_{VTT_PECL}	40	mW
P_{DEVICE}	948	mW

4.2 Driving the Clock Inputs

The AU5411 has two universal clock inputs (CLKin0/CLKin0* and CLKin1/CLKin1*). AU5411 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The AU5411 supports a wide common mode voltage range and input signal swing

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter.

It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say CLKin0, then CLKin0* pin need to be connected to a 0.1 uF capacitor on the PCB.

4.2.1 Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 5 shows how a differential input can be wired to accept LVCMOS single ended levels in AC coupled mode. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass should be located as close to the input pin as possible. Two resistors R_{T1} and R_{T2} set the common mode voltage at the output of the LVCMOS driver to $V_{CC}/2$. This prevents average DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{T1} and R_{T2} values should be adjusted to set the V1 at 1.25 V. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm$$

$$\frac{VCC * R_{T2}}{R_{T1} + R_{T2}} = \frac{VCC}{2}$$

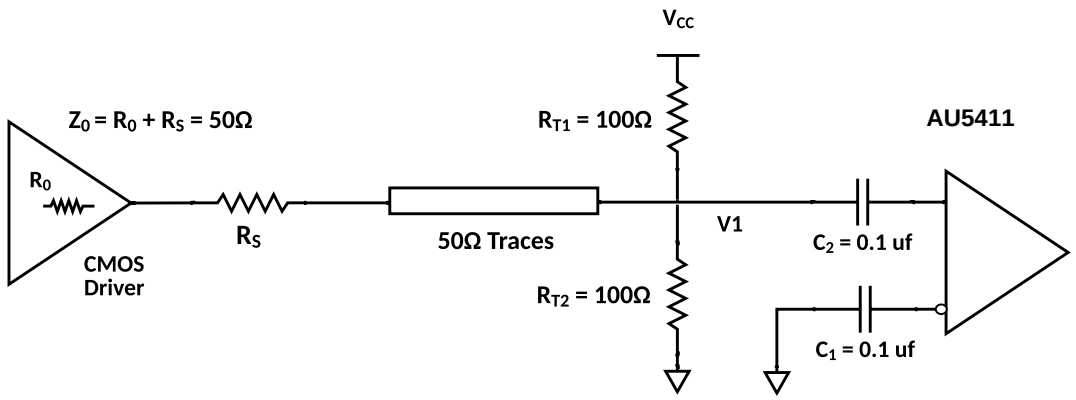


Figure 5 AC coupling LVCMOS clock to AU5411

The inverting differential input can be connected to a 0.1 uF bypass capacitor. This pin is biased internally to a voltage close to VCC/2.

Another variant of the AC coupling of LVCMOS input clock is shown in Figure 6. We use single termination resistor of 50 Ω to ground. A 0.1 uF (C_3) ac coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50\ Ohm$$

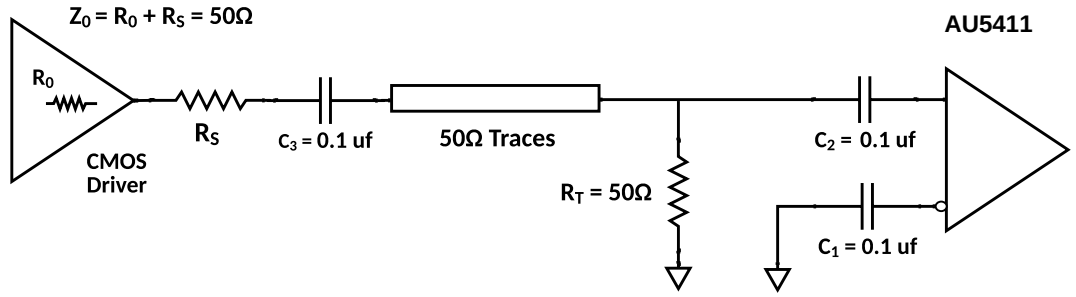


Figure 6 AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

4.2.2 Driving Clock Inputs with LVCMOS Driver (DC coupled)

Figure 7 shows how a differential input can be wired to accept LVCMOS single ended clock signals in DC coupled mode. The reference voltage V1 = VCC/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{VCC * R_{s2}}{R_{s1} + R_{s2}} = \frac{VCC}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm$$

$$\frac{VCC * R_{T2}}{R_{T1} + R_{T2}} = \frac{VCC}{2}$$

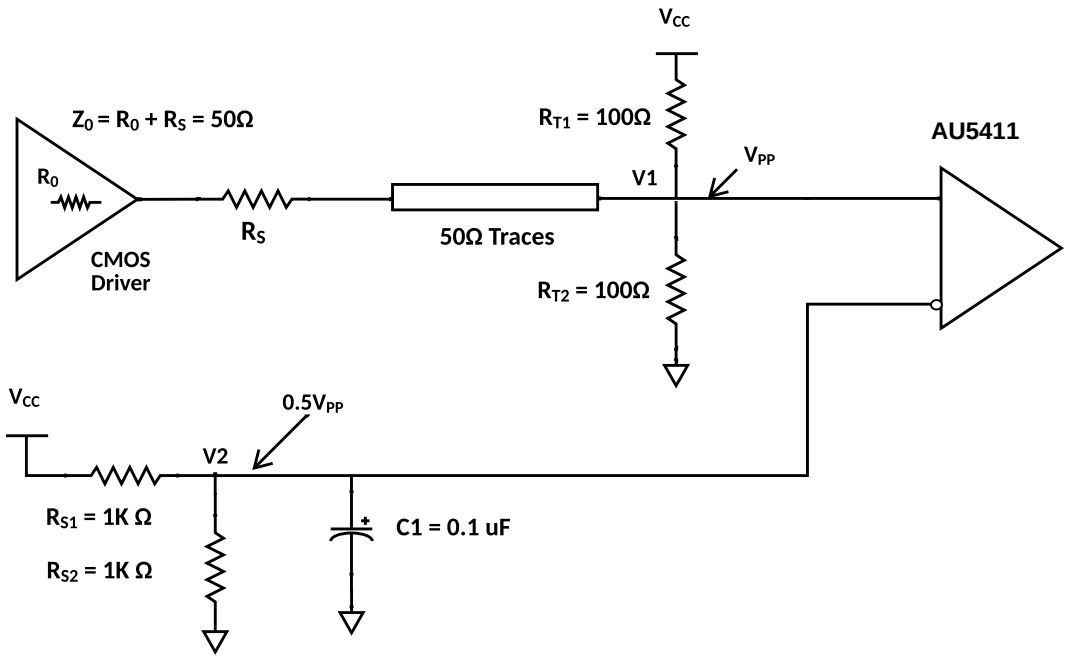


Figure 7 DC coupling of LVCMOS clock to AU5411 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values given below are for when both the single ended swing and VCC are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 8 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50 Ω load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 8 is given below

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{VCC * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2}$$

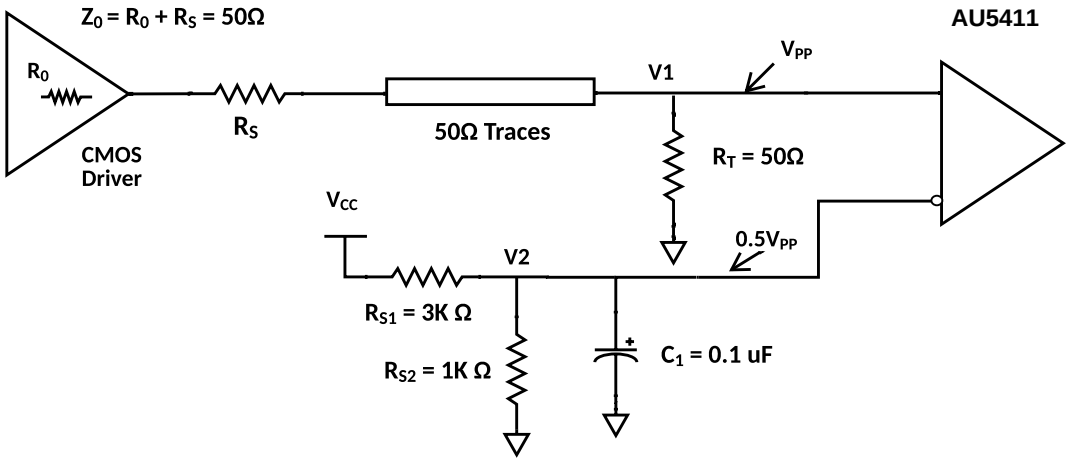


Figure 8 DC coupled LVCMOS input clock configuration – configuration 2

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 9. There is a single termination resistor RT which is connected to ground through a capacitor C_{AC}. The value of series capacitor is given by a formula.

$C_{AC} \geq \frac{3T_D}{50\Omega}$, T_D is the transmission line delay

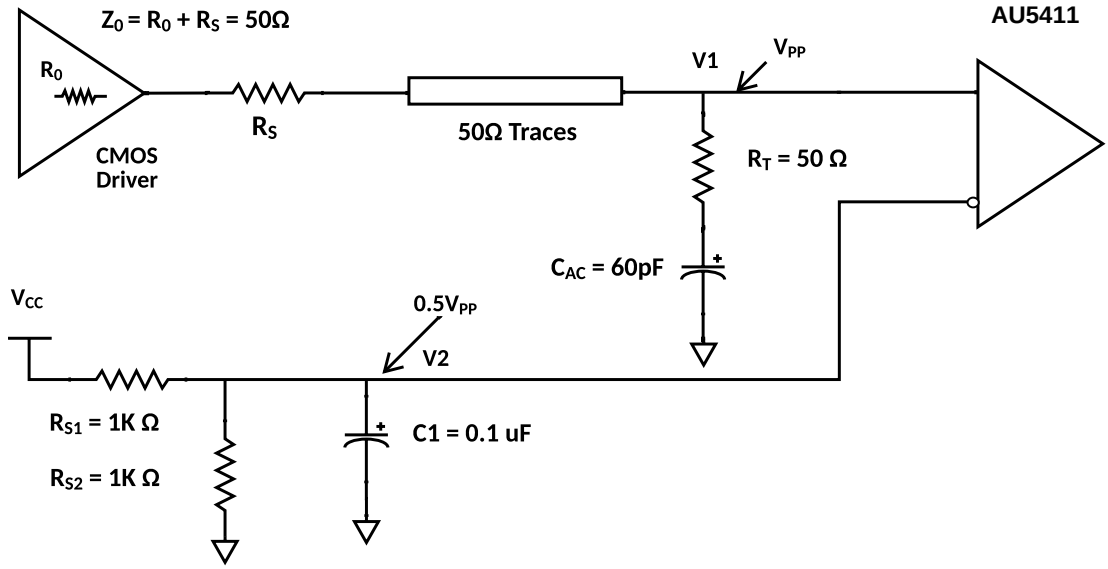


Figure 9 DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can direct couple the LVCMOS clock to AU5411 input clock pin as shown in Figure 10.

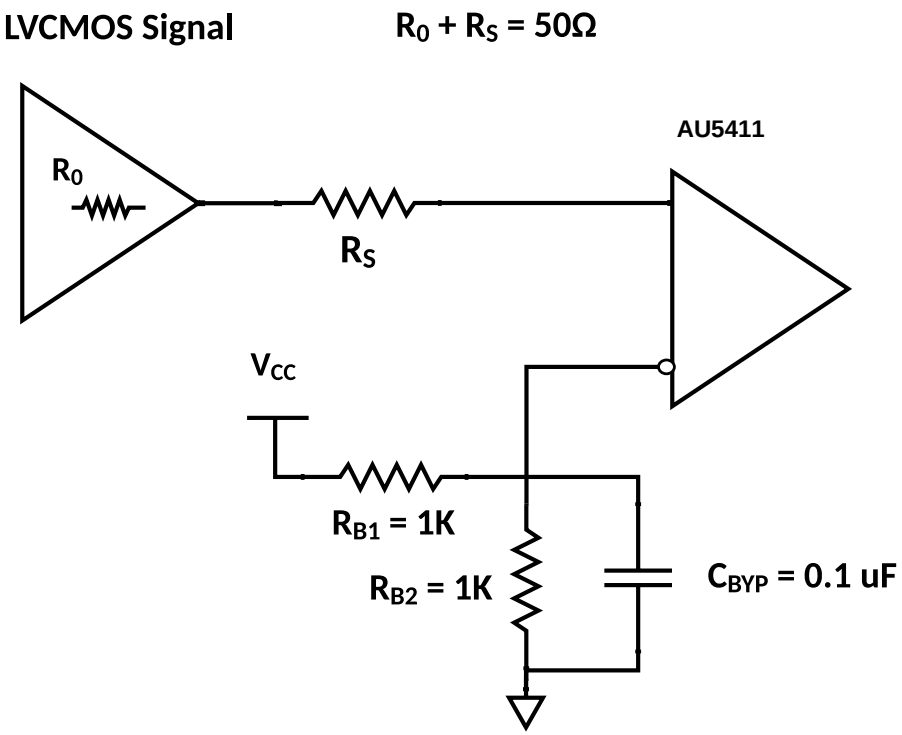


Figure 10: Direct coupling of LVCMOS clock to AU5411

4.2.3 Driving OSC_IN with LVCMOS Driver (AC coupled)

The crystal input OSC_IN can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at OSC_IN should be limited to 1.5 V. The OSC_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b10. The maximum voltage at OSC_IN should not exceed 1.5 V and minimum voltage should not go below -0.3 V. The slew rate at OSC_IN should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 11 shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm$$

$$\frac{VCC * R_{T2}}{R_{T1} + R_{T2}} = \frac{VCC}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.65 V. The maximum DC bias voltage of OSC_IN is 0.675 V. Therefore the maximum swing at the OSC_IN pin is given by the equation given below.

$$V_{swing,pk,XTAL\_IN} = 0.675 + 0.5 * 1.65 = 1.5V$$

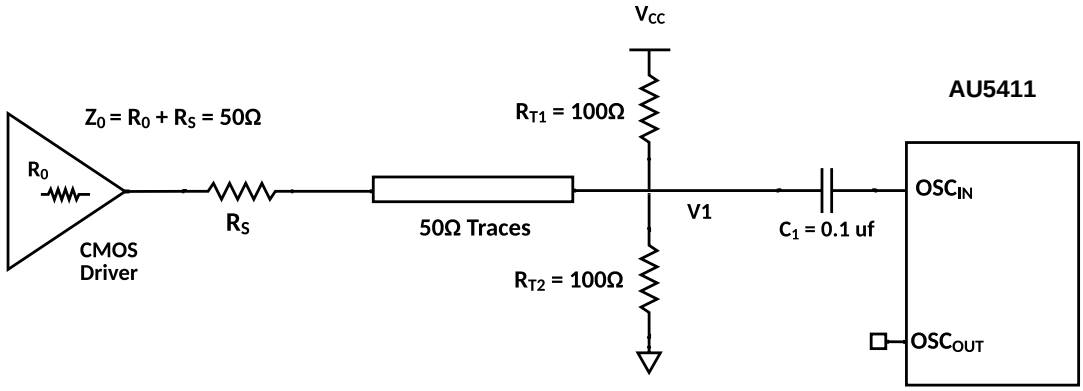


Figure 11 Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 12 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. A 0.1 uF is in series with the CMOS driver to prevent any DC leakage current.

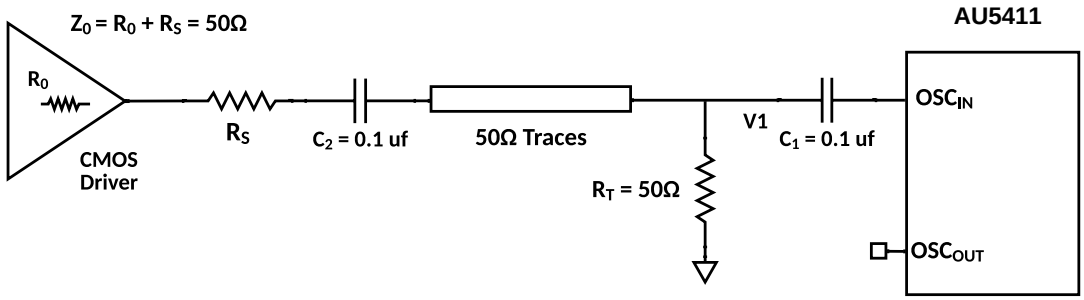


Figure 12 Single ended LVCMOS input – configuration 2, AC coupling to crystal input

4.2.4 Driving OSC_IN with LVCMOS Driver (DC coupled)

The crystal input OSC_IN can be overdriven with single ended clock as shown in Figure 13, in DC couple mode. The peak swing at OSC_IN should be limited to 1.5 V (voltage at the crystal input pin). The OSC_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b11. If the LVCMOS driver is on higher supply, say 3.3 V, use a resistor divider on the PCB to scale down the peak output voltage to 1.5 V.

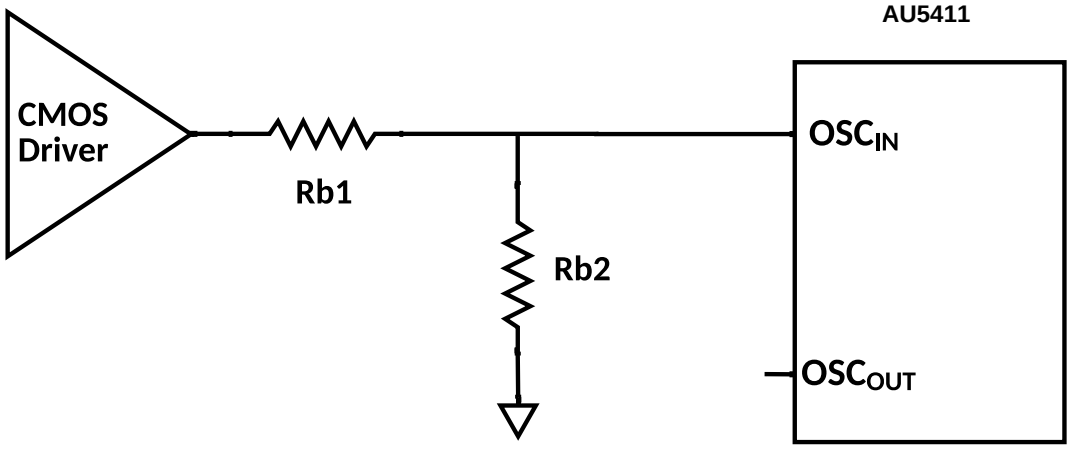


Figure 13 Single ended LVCMOS input, DC coupling to crystal input

4.2.5 LVDS (DC coupled)

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 14.

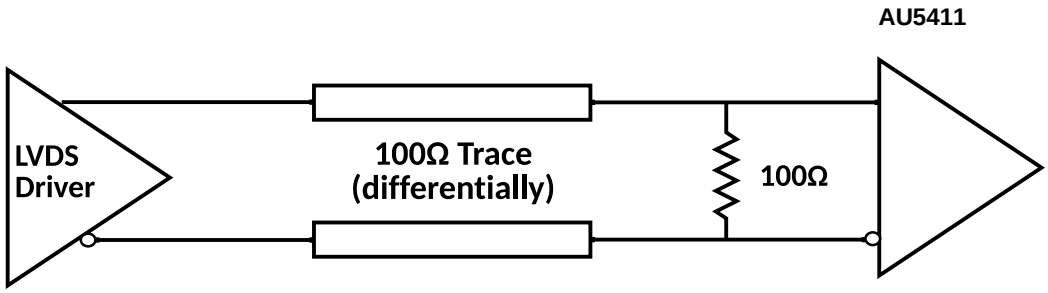


Figure 14 Termination scheme for DC coupled LVDS

4.2.6 HCSL (DC coupled)

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 15.

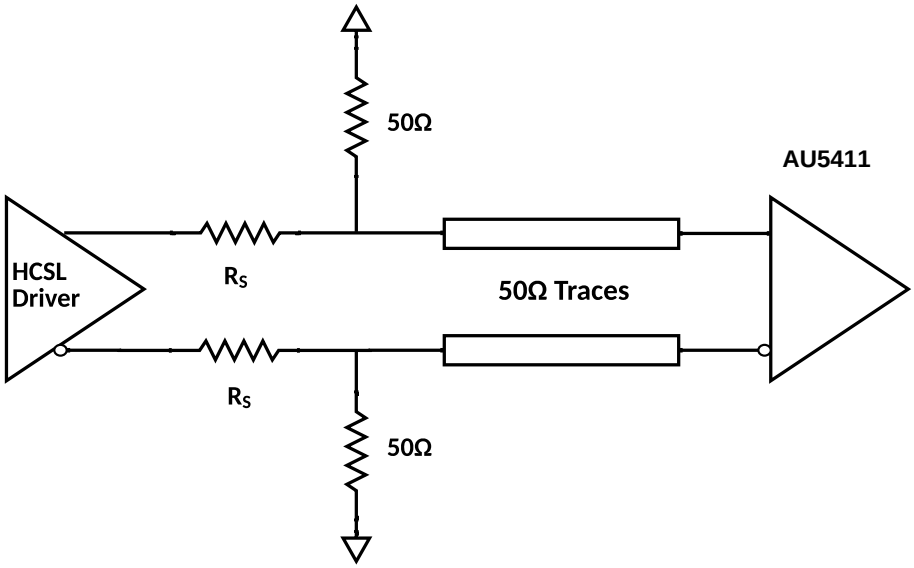


Figure 15 Termination scheme for DC coupled HCSL

4.2.7 LVPECL (DC coupled)

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source VTT.

$$V_{TT} = V_{CCO} - 2V.$$

This termination scheme is shown in Figure 16. Alternatively, the user can also implement a Thevenin equivalent of VTT using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 17

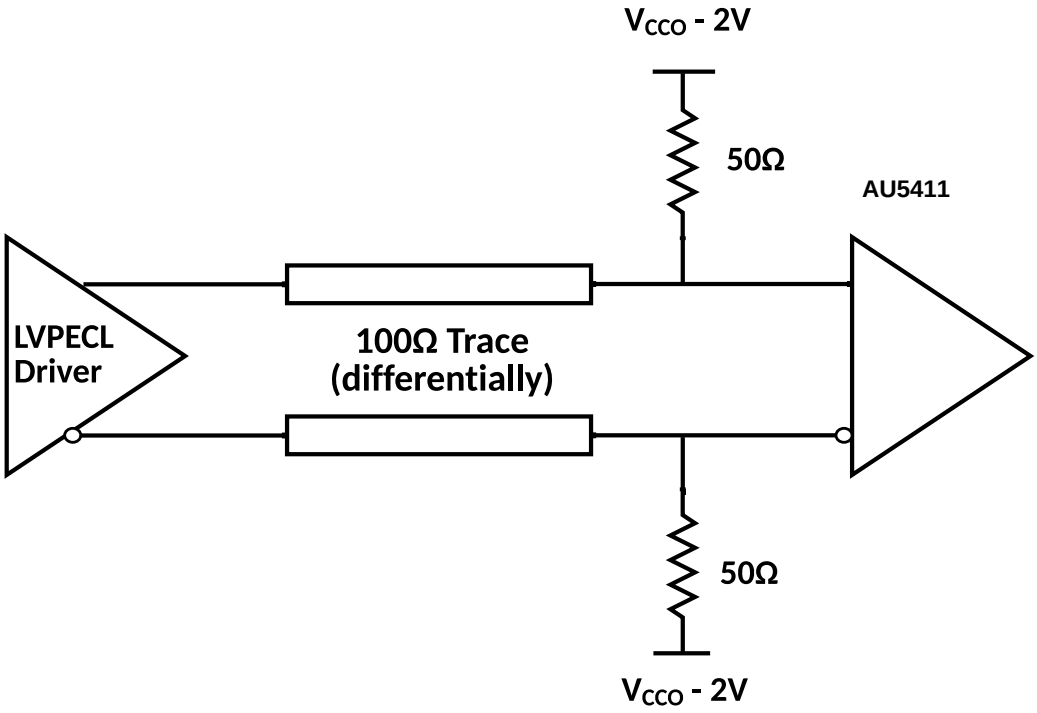
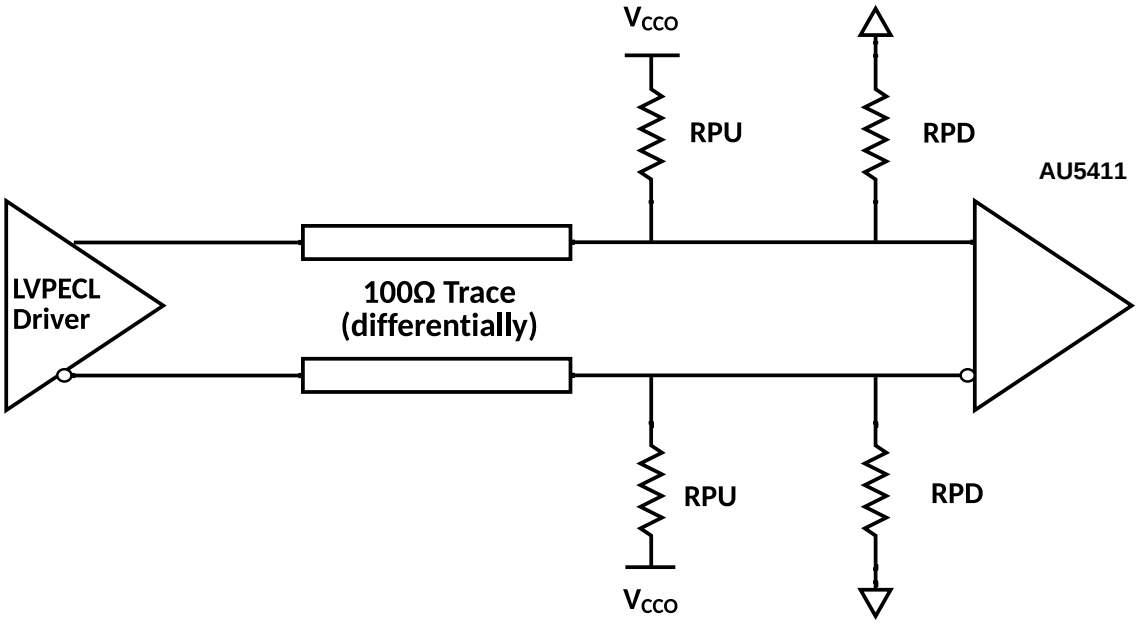


Figure 16 Termination scheme for DC coupled LVPECL



VCCO	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 17 Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * VCCO}{R_{PD} + R_{PU}} = VCCO - 2V$$

4.2.8 SSTL (DC coupled)

The SSTL input clock configuration is shown in Figure 18. The transmission line impedance is 60 Ω in the application example given. Therefore we use two 120 Ω resistors from VCCO to ground for biasing the clock input pins. The effective termination impedance in this case is 60 Ω.

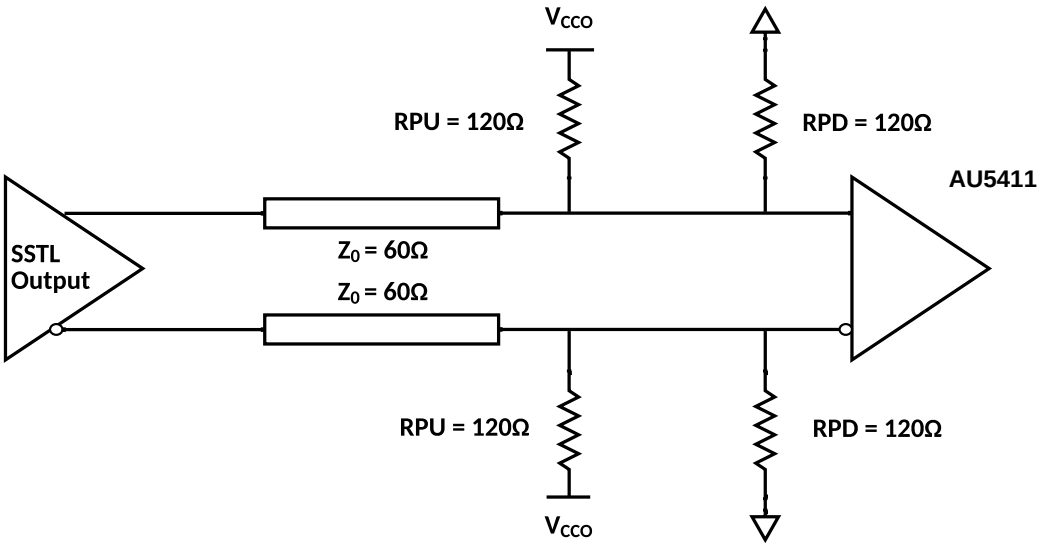


Figure 18 Example of input clock termination for SSTL clock.

4.2.9 LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 19.

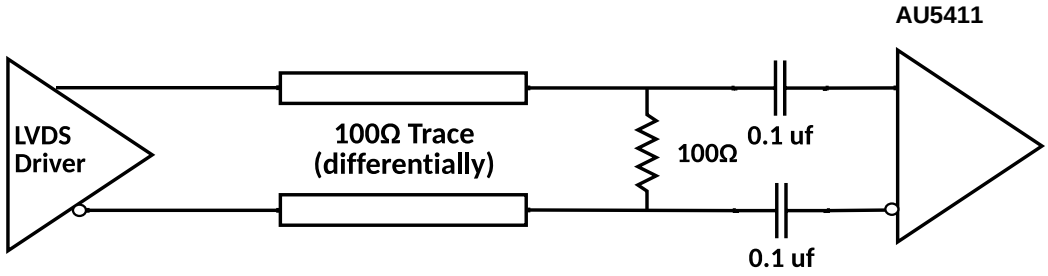


Figure 19 Termination scheme for AC coupled LVDS

4.2.10 LVPECL (AC coupled)

The LVPECL should have a DC path to ground. So, the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 20.

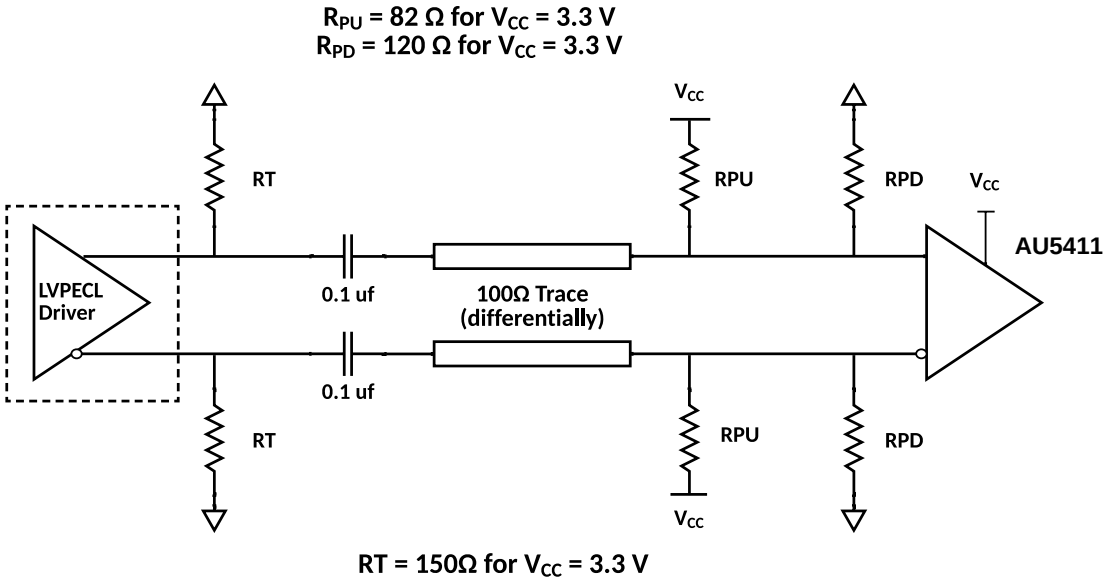


Figure 20 Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance RPU and pull down resistance RPD sets the input common mode voltage for AU5411.

The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{VCC * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The differential input common mode specification of AU5411 (from data sheet) is VCC -1.1 = 2.2 V, therefore the input common mode set by LVPECL AC coupled termination meets the AU5411 input common mode specification.

The LVPECL driver chip has resistance RT providing DC path for the output driver current in the LVPECL driver.

The effective load impedance at the input side of AU5411 (receiver side) is formed by parallel combination of RPU, RPD.

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

4.3 Termination of Output Driver of AU5411 for Various Load Configurations

4.3.1 AU5411 REFOUT Termination for AC Coupled mode

AC coupling of AU5411 LVCMOS output driver is shown in Figure 21. We use single termination resistor of 50 Ω to ground. A 0.1 uF AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single 50 Ω resistance to ground. The clock signal is then AC coupled to the receiver, in this example. C1 is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50\ Ohm$$

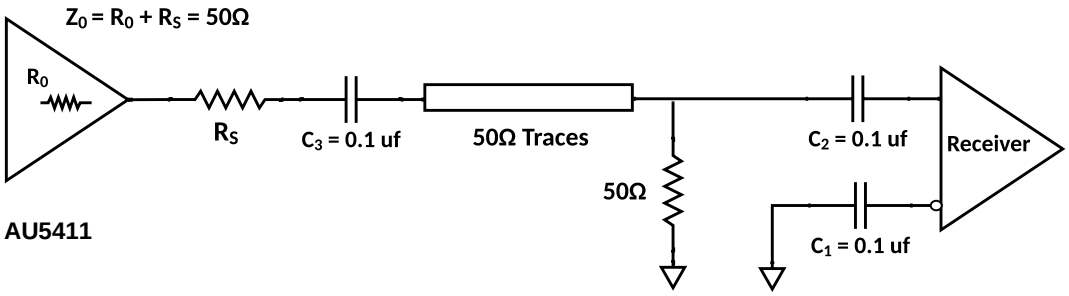


Figure 21 AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

4.3.2 AU5411 REFOUT Termination for DC Coupled mode

Figure 22 shows how AU5411 LVCMOS output drive can be terminated to send clock signals in DC coupled mode. The reference voltage V1= VCC/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C_1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{VCC * R_{s2}}{R_{s1} + R_{s2}} = \frac{VCC}{2}, Typical\ value\ of\ R_{s1} = R_{s2} = 1K\Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm, Typical\ value\ of\ R_{T1} = R_{T2} = 100\Omega$$

$$\frac{VCC * R_{T2}}{R_{T1} + R_{T2}} = \frac{VCC}{2}$$

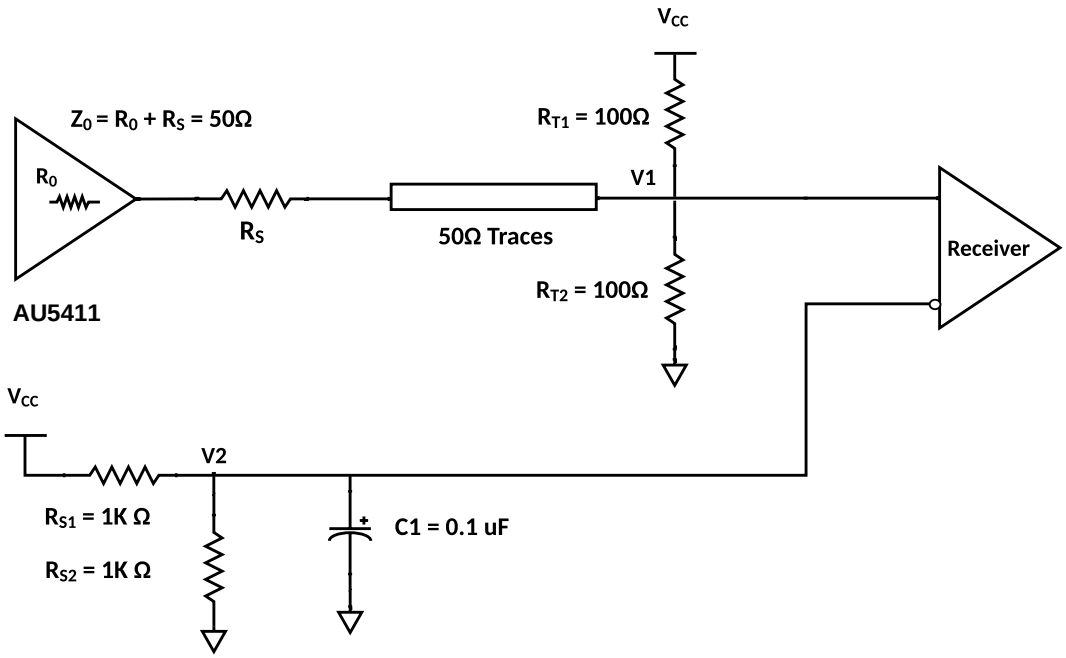


Figure 22 DC coupling of LVCMOS output clock termination – configuration 1

For example, if the AU5411 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values given below are for when both the single ended swing and VCC are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 23 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor R_T to ground. There will be DC leakage current from AU5411, for the output termination shown in Figure 23. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 23 is given below

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{VCC * R_{s2}}{R_{s1} + R_{s2}} = \frac{VPP}{2} = \frac{VCC}{4}, Typical\ value\ of\ R_{s1} = 3K\Omega, R_{s2} = 1K\Omega$$

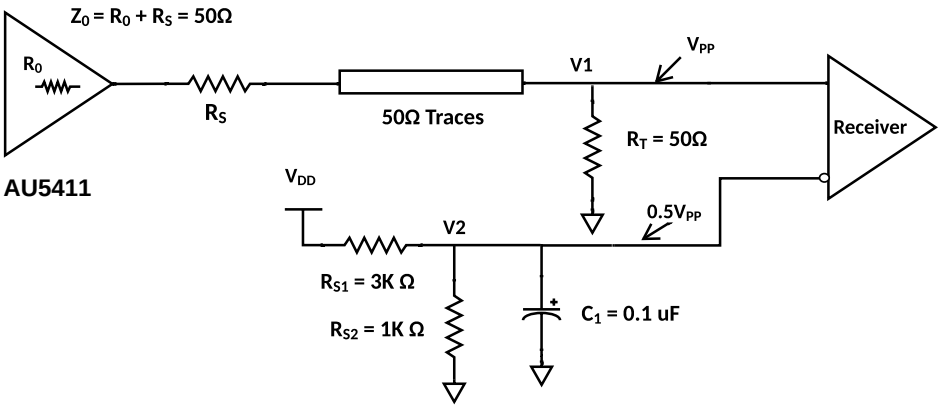


Figure 23 DC coupled LVCMOS output clock configuration – configuration 2

The AU5411 LVCMOS output driver termination with series RC termination near the buffer is shown in Figure 24. There is a single termination resistor RT which is connected to ground through a capacitor C_{AC}. The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega},\ T_D \text{ is the transmission line delay}$$

Typical value for C_{AC} is 60 pF, assuming delay of T_D = 200 ps/inch and 5 inch input clock route length.

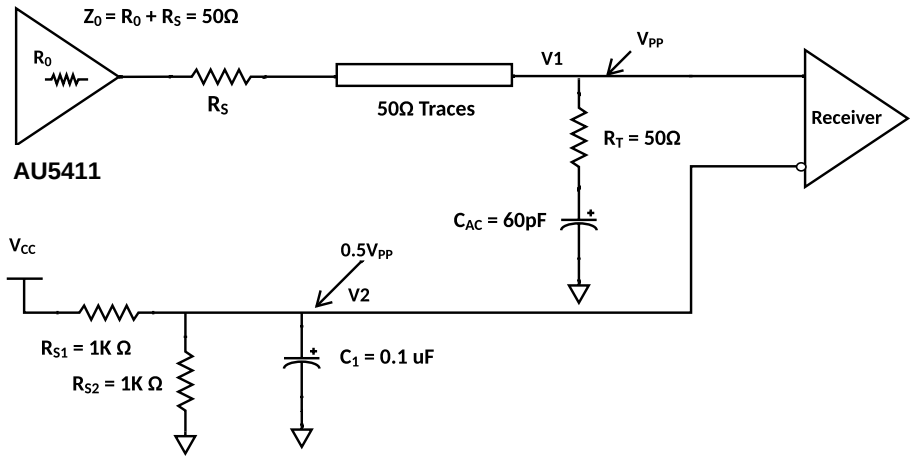


Figure 24 DC coupled LVCMOS output clock with series RC termination – configuration 3

The typical value of R_{S1} and R_{S2} in this case is 1K Ω and that of C_{AC} is 60 pF.

4.3.3 CMOS (Capacitive load)

The capacitive load can be driven as shown in figure below. For AU5411 LVCMOS driver the Ro is very close to 50 Ω by design. Therefore Rs = 0 Ω is recommended.

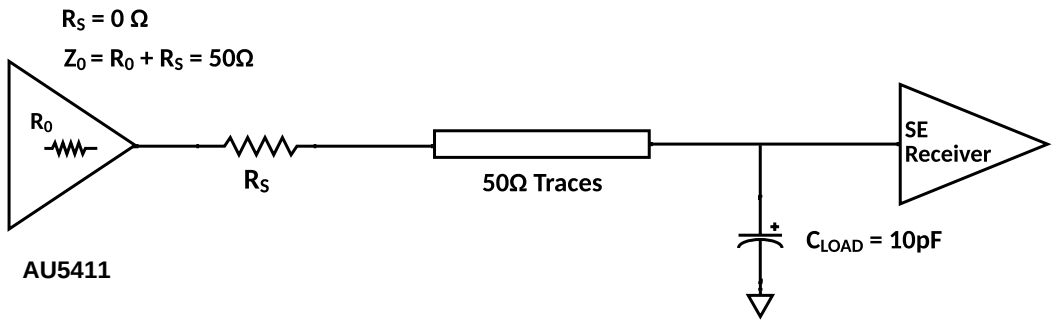


Figure 25 Typical application load

4.4 Termination of Output Drivers (DC coupled)

4.4.1 LVDS DC Coupled Output Termination

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 26.

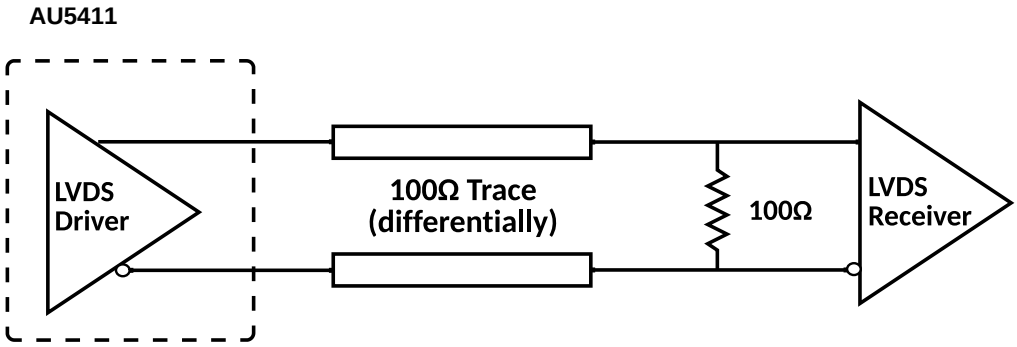


Figure 26 Termination scheme for DC coupled LVDS

4.4.2 HCSL DC Coupled Output Termination

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 27.

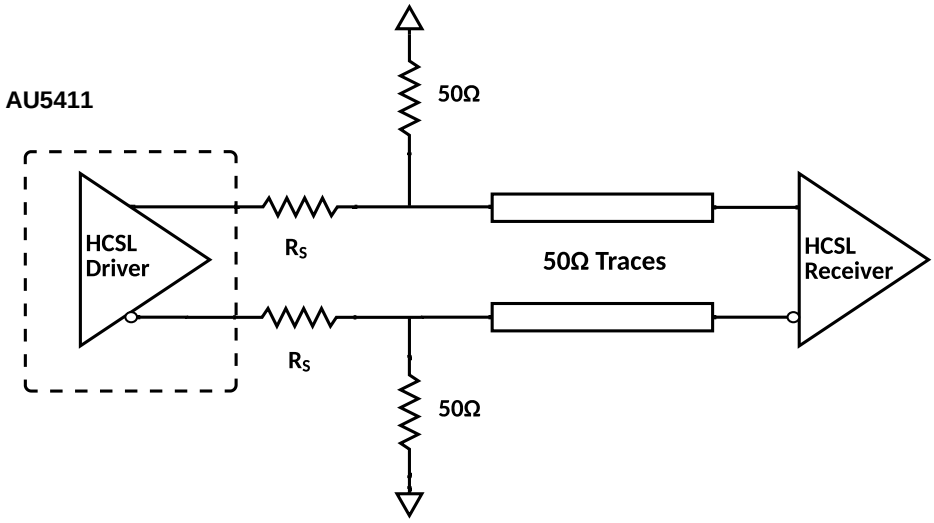


Figure 27 Termination scheme for DC coupled HCSL

4.4.3 LVPECL DC Coupled Output Termination

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source VTT. Typically, $V_{TT} = V_{CCO} - 2V$.

This termination scheme is shown in Figure 28. Alternatively, the user can also implement a Thevenin equivalent of VTT using a resistor divider.

This scheme and the values of the resistors in the resistor divider are given in Figure 29.

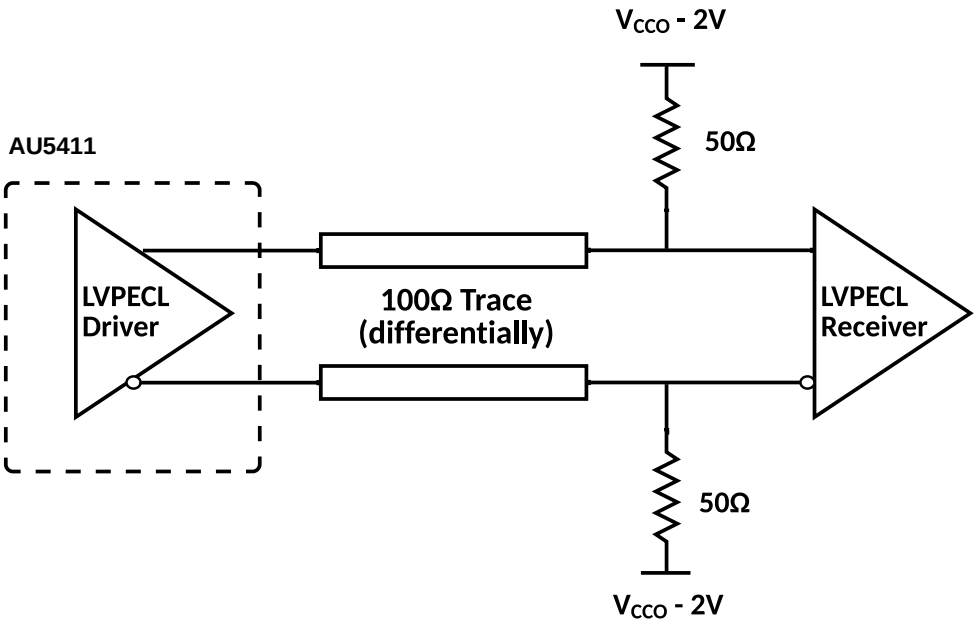
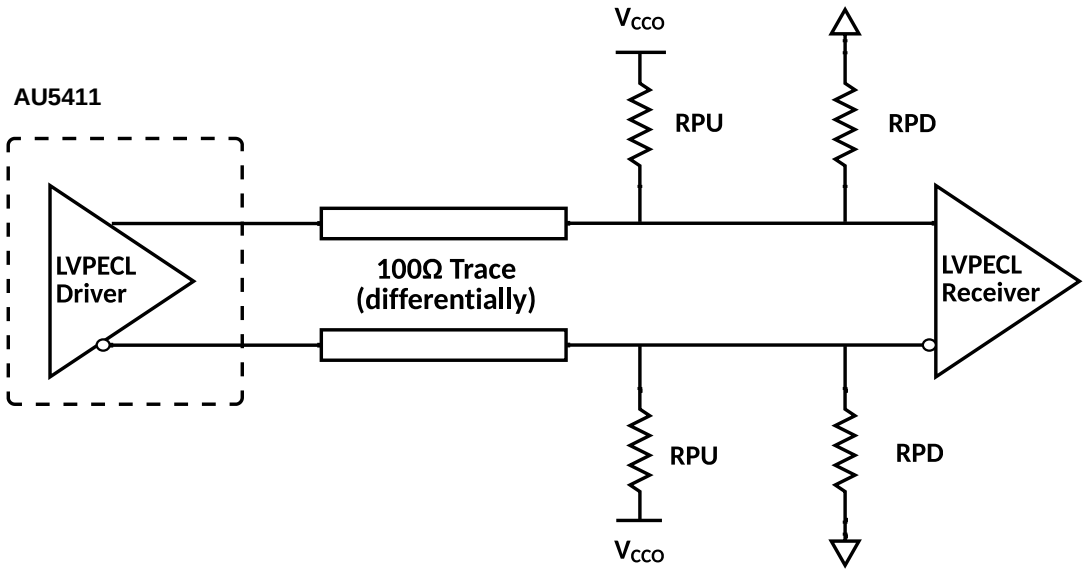


Figure 28 Termination scheme for DC coupled LVPECL

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * VDDO}{R_{PD} + R_{PU}} = VCCO - 2V$$



VCCO	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 29 Termination scheme for DC coupled LVPECL, Thevenin equivalent

4.5 Termination of Output Drivers (AC coupled)

4.5.1 LVDS AC Coupled Output Termination

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 30. First figure shows AU5411 output driver configured in LVDS mode. The receiver in this case is shown as LVDS receiver. The second figure shows AU5411 output driver configured in LVDS mode and the receiver in this case is shown as CML receiver. As long as the LVDS swing is okay with the recevire the AC coupled output termination is same.

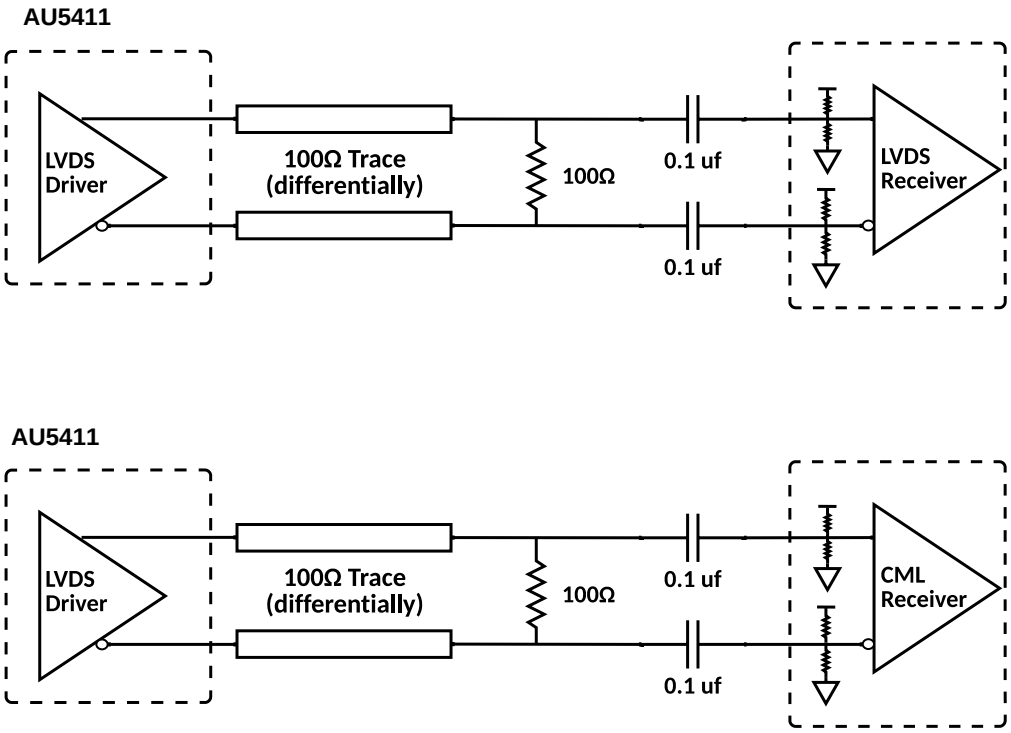


Figure 30 Termination scheme for AC coupled LVDS, driving LVDS receiver and CML receiver

4.5.2 LVPECL AC Coupled Output Termination

The LVPECL should have a DC path to ground. So the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 31. AU5411 swing reduces by about 20% as the effective load resistor is now the parallel combination of RT at the driver side and 50 Ω at the receiver side.

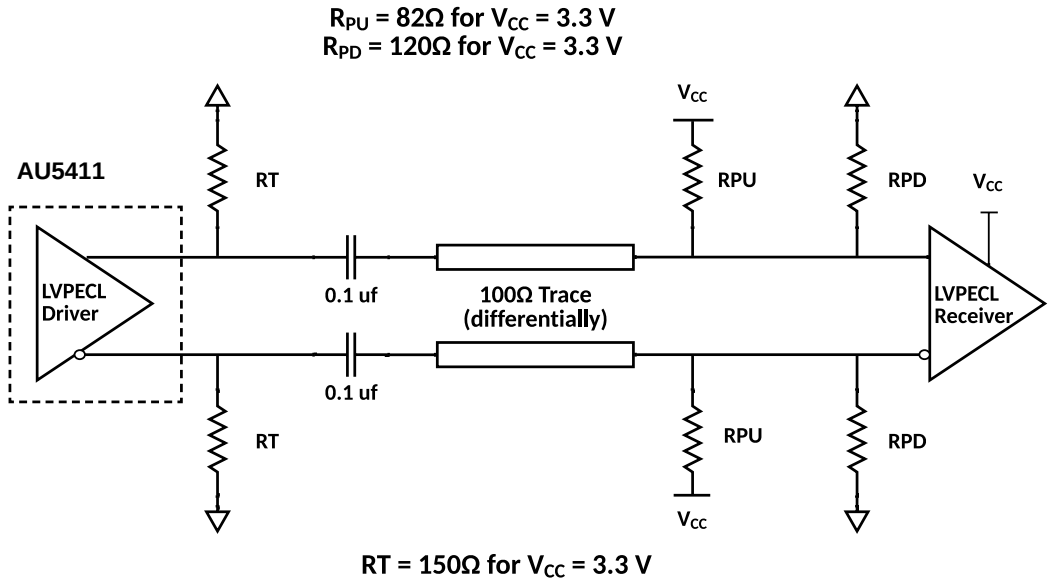


Figure 31 Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance RPU and pull down resistance RPD sets the input common mode voltage for LVPECL receiver.

The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{VCC * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The LVPECL driver of AU5411 has resistance RT providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the receiver side is formed by parallel combination of RPU, RPD. The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

4.5.3 Termination of Output Drivers in LVPECL Mode, Single Ended, DC coupled

Single ended LVPECL operation is possible. The user can use a balun to convert differential output to single ended output. It is also possible to use the LVPECL driver as one or two separate 700 mV - PP signal. The unused output need to be terminated close to the output driver.

These termination schemes are shown in Figure 32 and Figure 33.

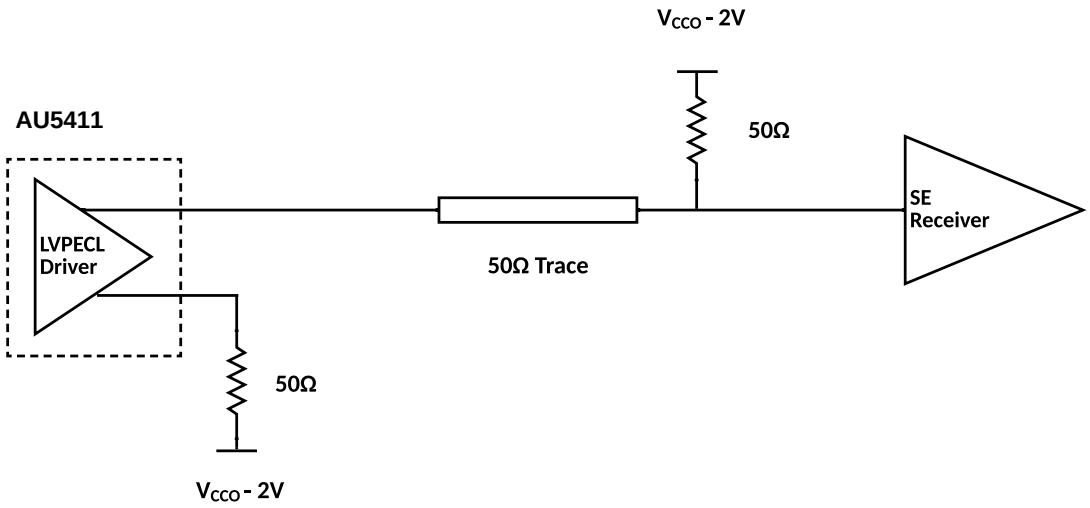
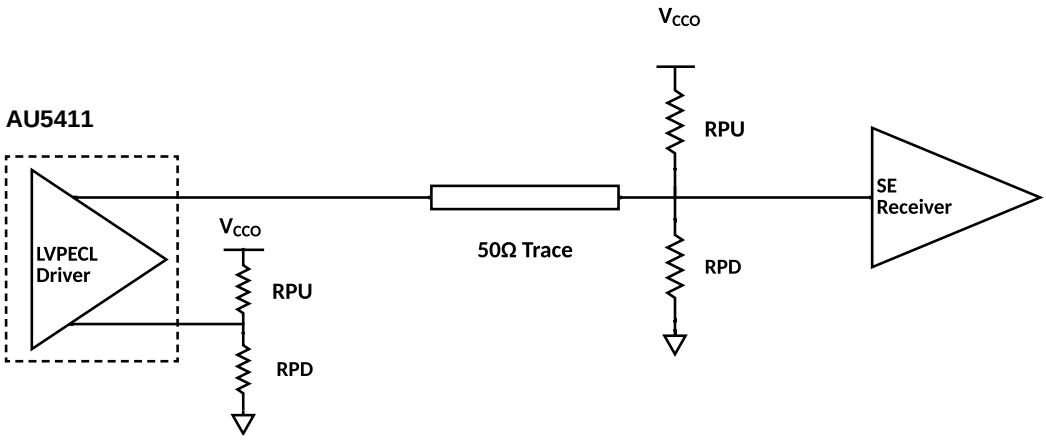


Figure 32 Termination scheme for DC coupled LVPECL, single ended

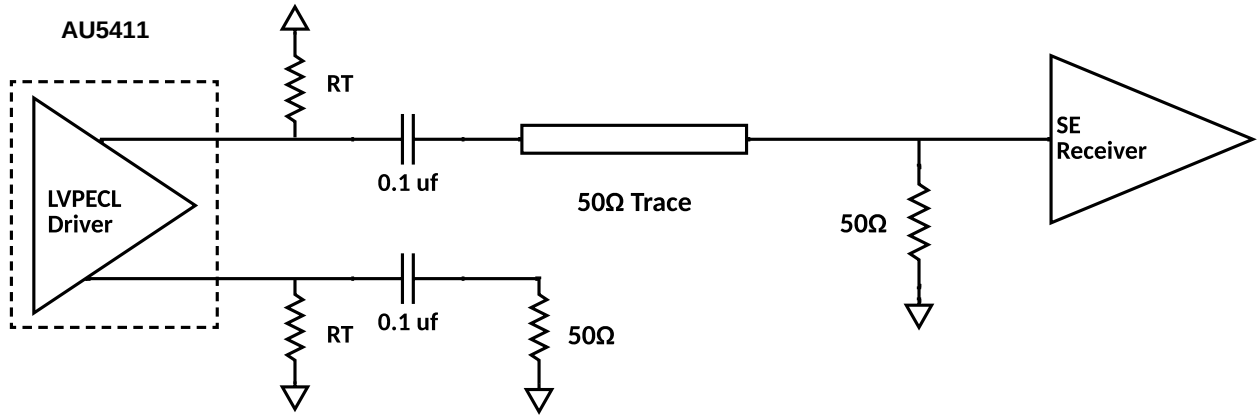


VCCO	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 33 Termination scheme for DC coupled LVPECL, single ended, Thevenin equivalent

4.5.4 Termination of Output Drivers in LVPECL Mode, Single Ended, AC coupled

LVPECL output driver needs a DC path to ground from its output. Therefore 160 Ω (if V_{CC} = 3.3 V) resistor to ground is connected from the output of the LVPECL driver to ground. If V_{CC} = 2.5 V, the DC path resistance should be 91 Ω. The 50 Ω load termination resistor must be placed close to input receiver and biased to a suitable voltage.



VCCO	RT
3.3 V	160 Ω
2.5 V	91 Ω

Figure 34 Termination scheme for AC coupled LVPECL, single ended

4.5.5 Termination of Output Drivers in AC coupled HCSL mode

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. AC coupling capacitor of 0.1 uF is used to couple the output HCSL signal in to the receiver. The same termination can be used for CML receiver.

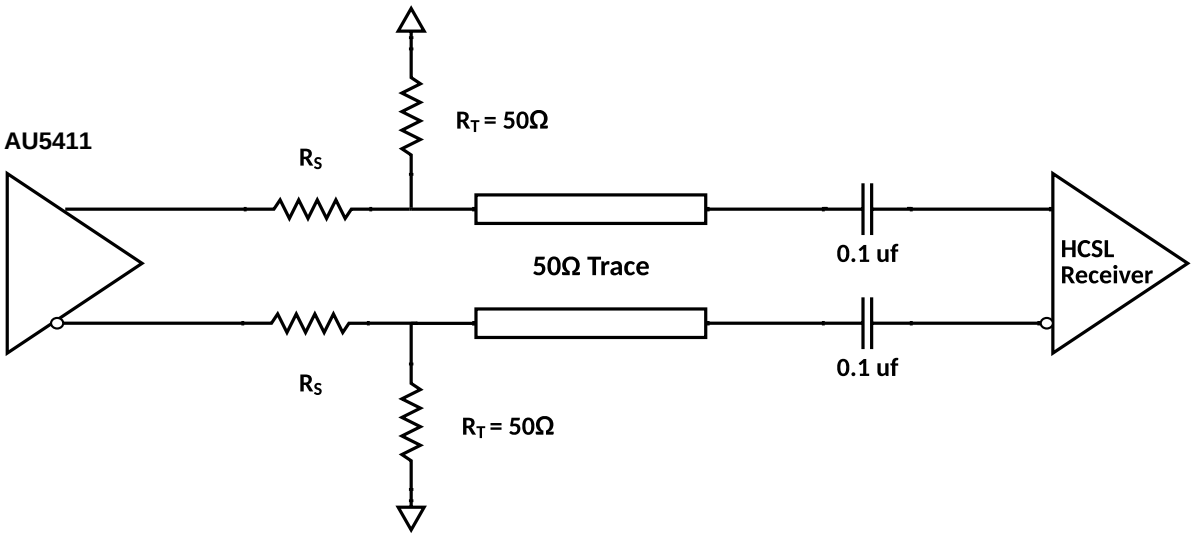


Figure 35 Output driver termination in HCSL AC coupled mode

5 Thermal Information

Table 16 Thermal Metrics of AU5411

Thermal Metric	AU5411 RHB 32 pins	Units
θ_{JA} Junction to ambient thermal resistance, flow = 0 m/s	36.3	°C/W
θ_{JA} Junction to ambient thermal resistance, flow = 1 m/s	31.6	°C/W
θ_{JA} Junction to ambient thermal resistance, flow = 2 m/s	30.4	°C/W
θ_{JB} Junction to board	15.21	°C/W
θ_{JC} Junction to case	18.90	°C/W
ψ_{JT} Junction to top characterization parameter	0.63	°C/W

6 HOT Swap Recommendations

6.1 Introduction

Hot-swap is a term used to refer to the insertion and removal of a daughter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can be damaged.

6.2 Typical Differential Input Clock

For example, Figure 36 shows a typical LVPECL driver and differential input. If the power of the driver (V_{CCO}) is turned on before the input supply (V_{CCI}), there is a possibility that the input current could exceed the limit and damage diode D1.

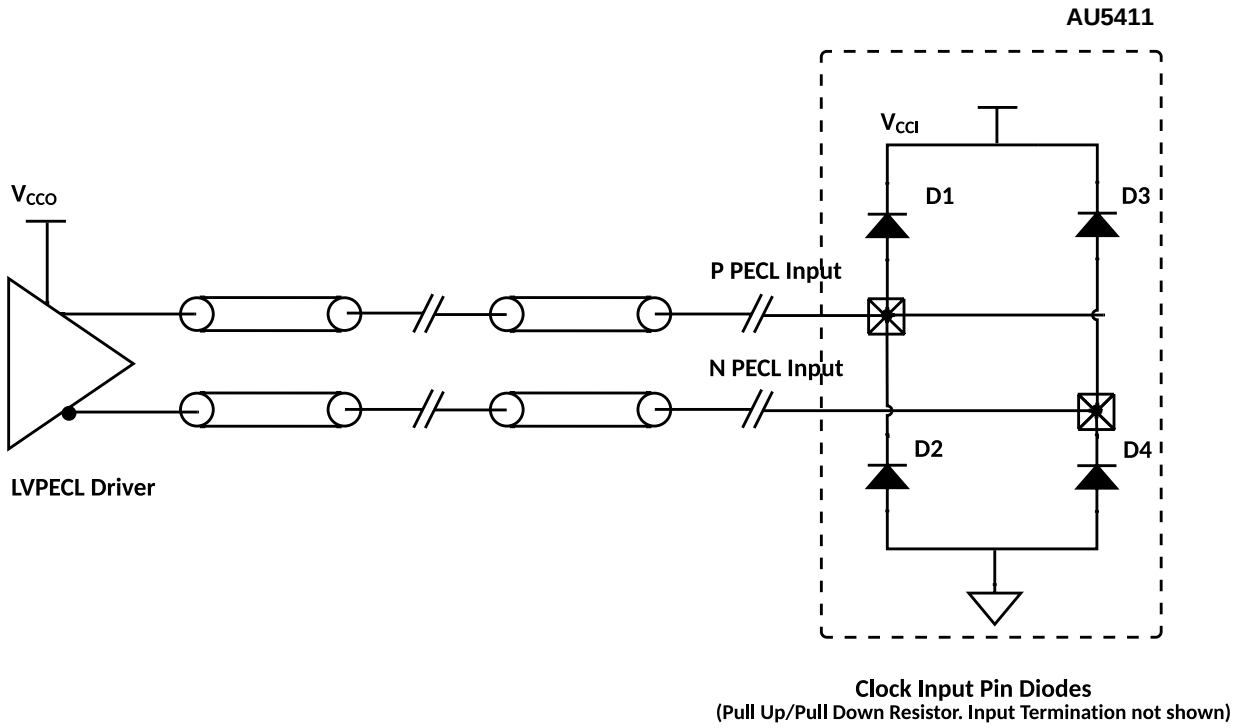


Figure 36 Typical input differential clock

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though it's not necessary, but if board space allows, some of the examples have an optional 100pf capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible.

6.3 Input Clock Termination with Hot Swap Protection

6.3.1 LVPECL Termination Example

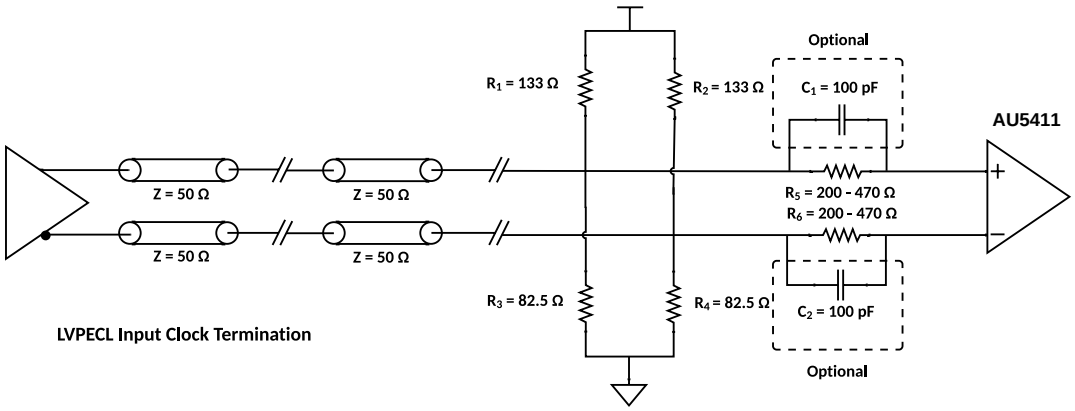


Figure 37 LVEPCL termination with hot swap protection

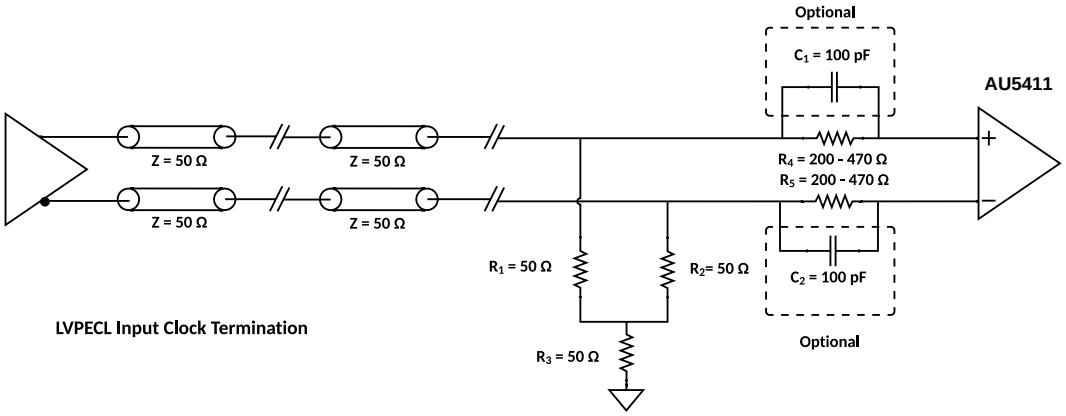


Figure 38 LVPECL termination with hot swap protection

6.3.2 LVDS Input Clock Termination Example

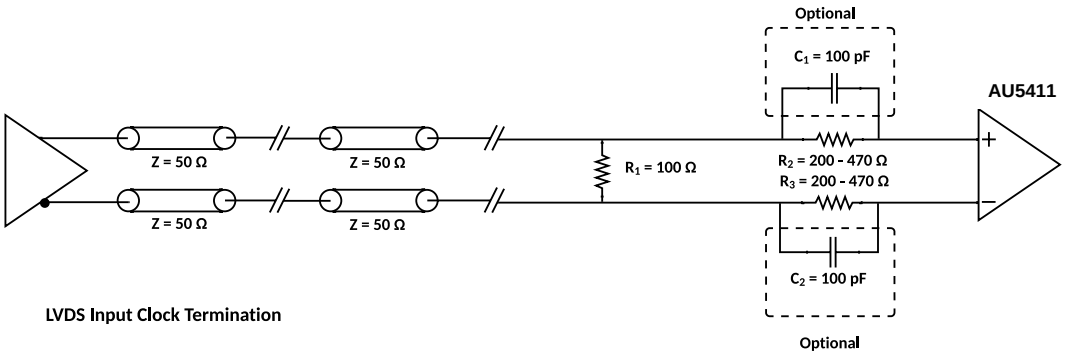


Figure 39 LVDS termination with hot swap protection

6.3.3 HCSL Input Clock Termination Example

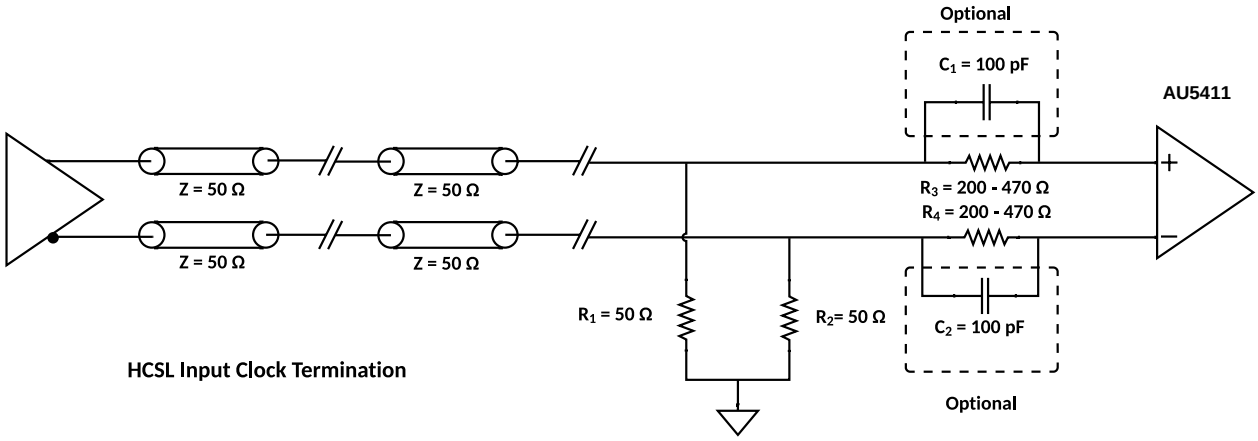


Figure 40 HCSL termination with hot swap protection

6.3.4 LVCMOS Input Clock Termination with Hot Swap Protection

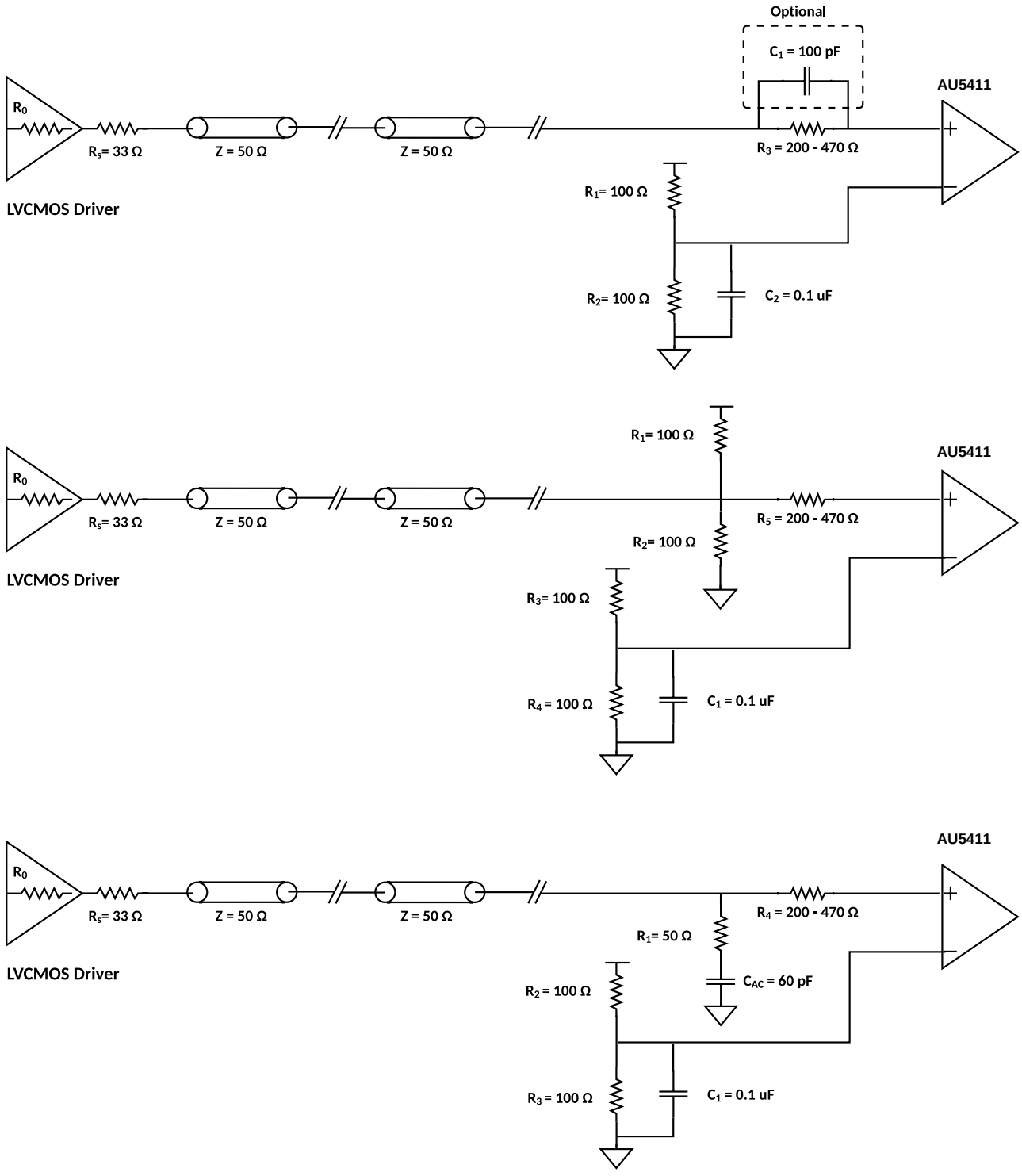


Figure 41 LVCMOS input clock termination with hot swap protection

6.4 LVCMOS Output Clock Termination with Hot Swap Protection

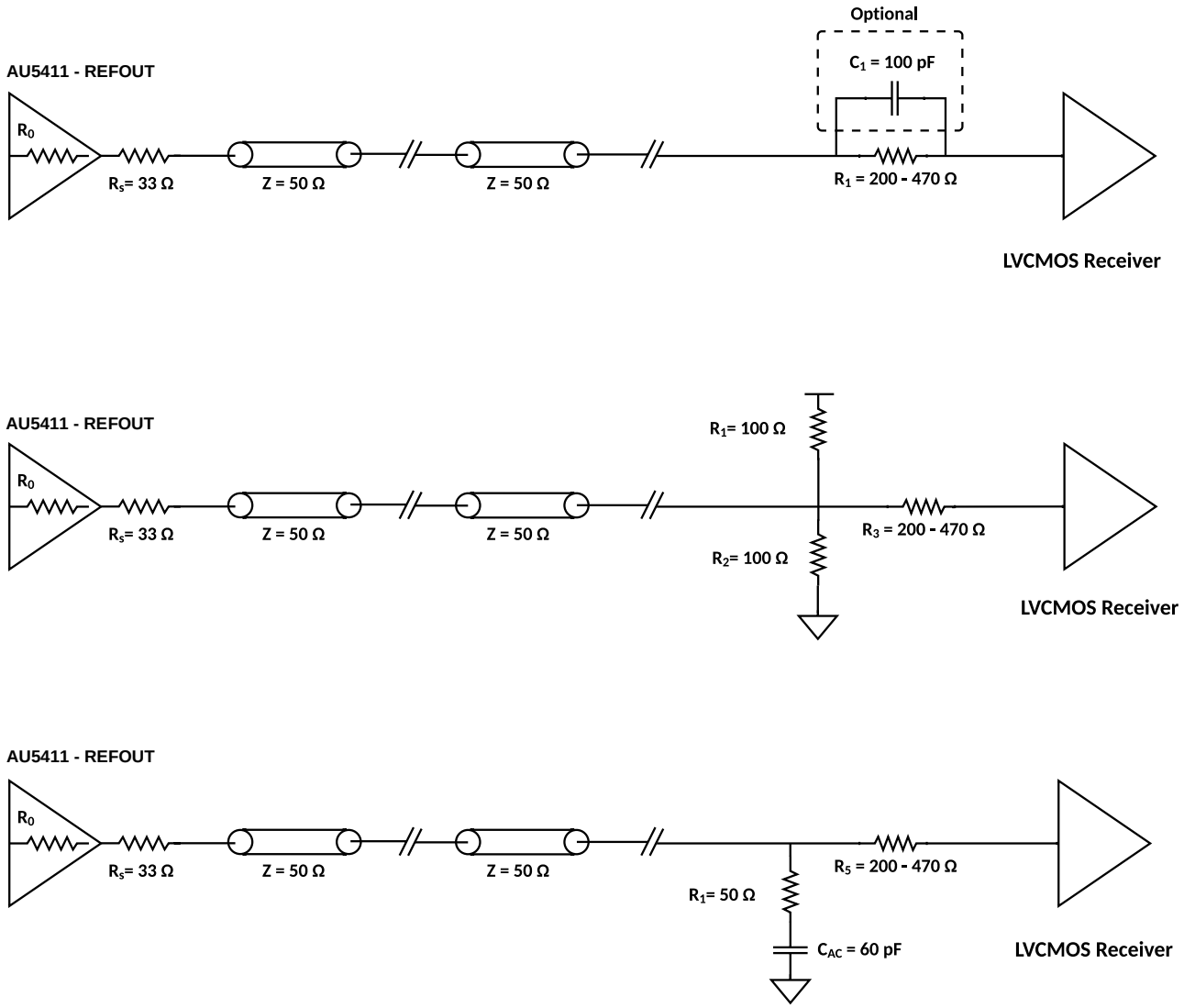


Figure 42 Different types of LVCMOS output clock termination with hot swap protection.

7 Parameter Measurement Information

7.1 Differential Input Level

The parameter definitions related to differential input level is shown below.

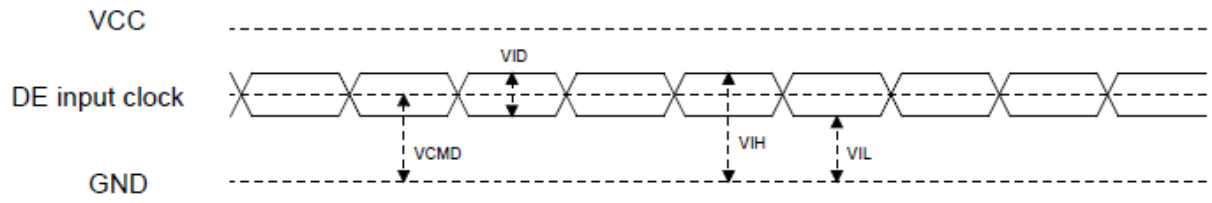


Figure 43 Parameters related to differential input level

7.2 Differential Output Level

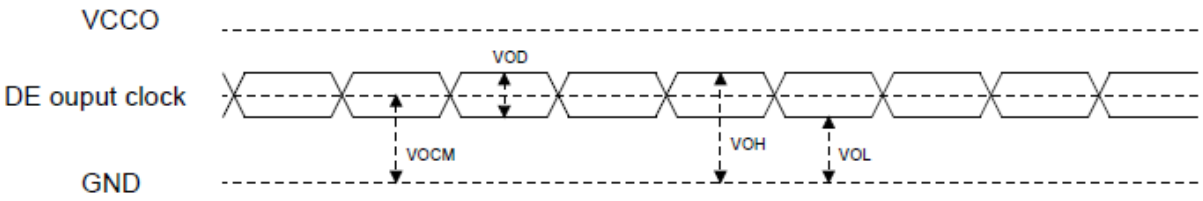


Figure 44 Parameters related to differential output clock levels

7.3 Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown below.

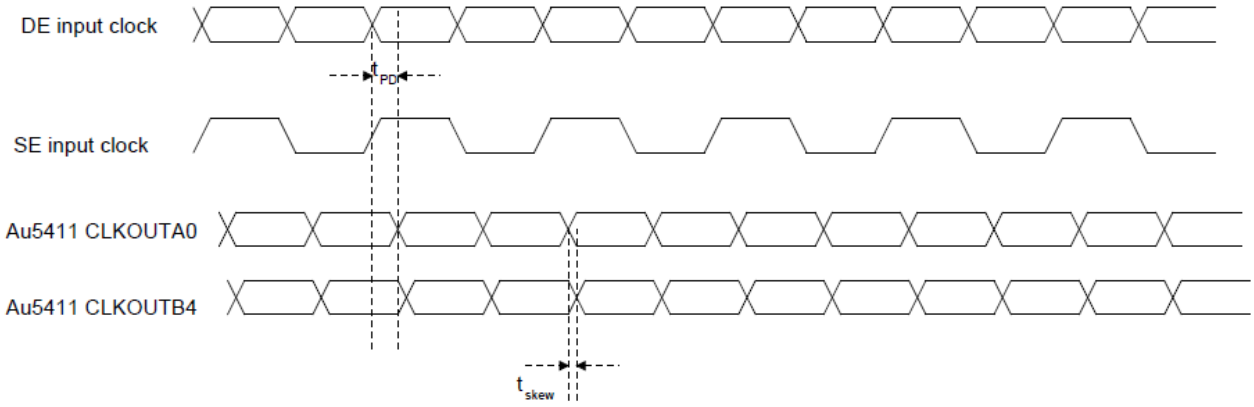


Figure 45 Parameter definitions of propagation delay and skew

7.4 Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown below.

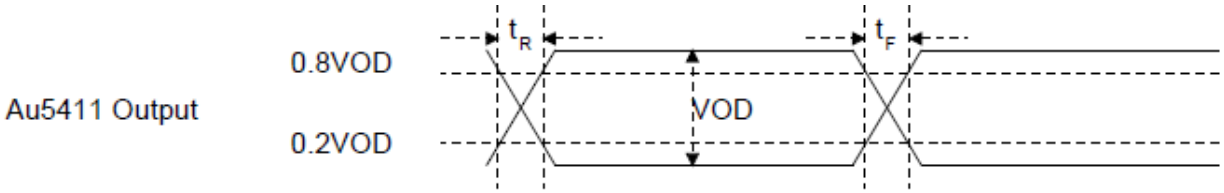


Figure 46 Parameter definitions related to rise and fall times

7.5 Isolation

Isolation is a measure of the coupling of clock toggling in unselected input clock path on the output clock. Let us say that CLOCK0 path is selected and there the clock frequency is 156.5 MHz at 0 dBm power. If a clock is toggling in CLOCK1 path at 156 MHz at 0 dBm, then we there may be a tone at an offset of 0.5 MHz from the carrier, in the output clock. The power of this tone with respect to the carrier is called isolation.

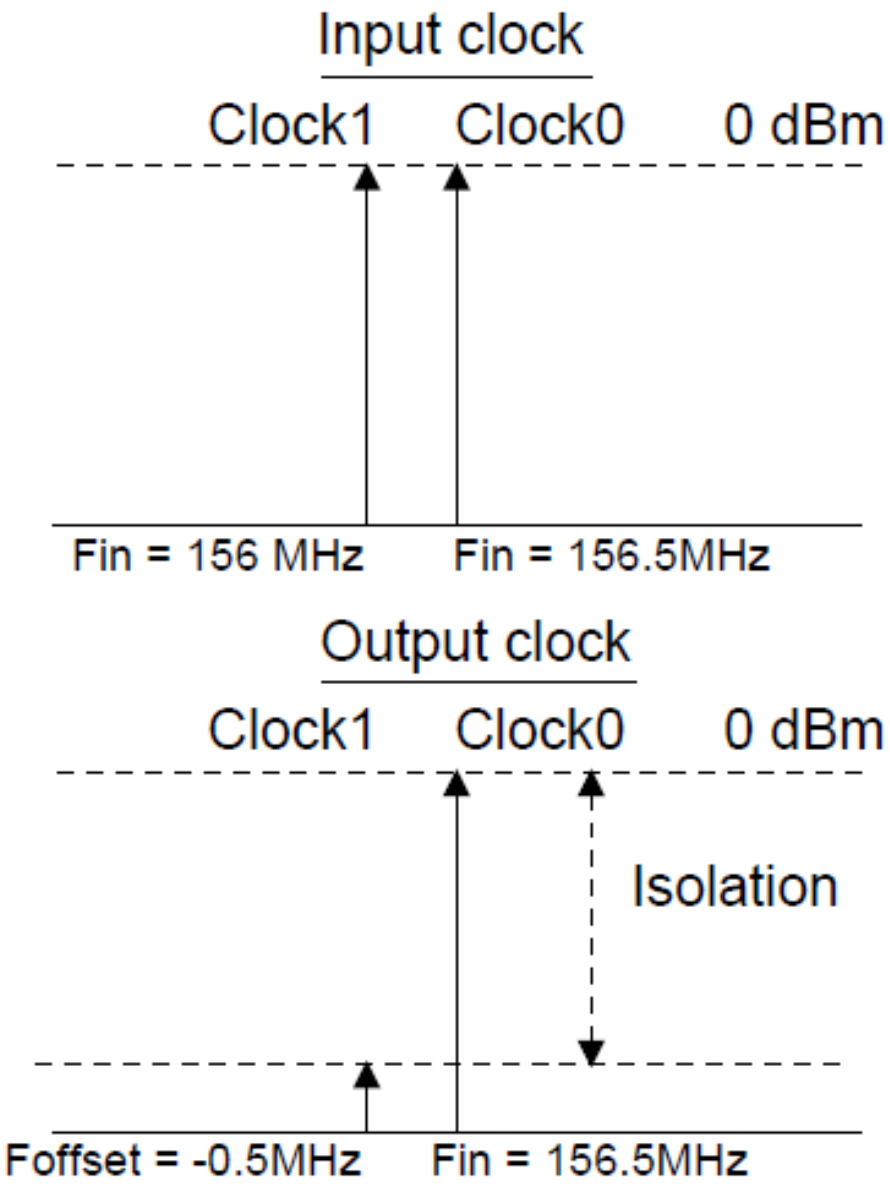


Figure 47 Parameter definition of isolation

7.6 Operation in Multiple VCCO Supply Domains

The VCCOA pins, 5 and 8 on the left side are shorted internally. These pins along with ODR $CLK_{OUT}A0$ to $CLK_{OUT}A4$ belong to a single supply domain. The VCCOB pins, 32 and 29 on the right side are shorted internally. These pins along with ODR $CLK_{OUT}B0$ to $CLK_{OUT}B4$ belong to a single supply domain. These two supply domains are totally independent of each other. Pin 5, 8 can be connected to say 3.3 V while pin 32, 29 can be connected to 2.5 V. In this example, $CLK_{OUT}A0$ to $CLK_{OUT}A4$ will be 3.3 V output driver. $CLK_{OUT}B0$ to $CLK_{OUT}B4$ will be 2.5 V output driver.

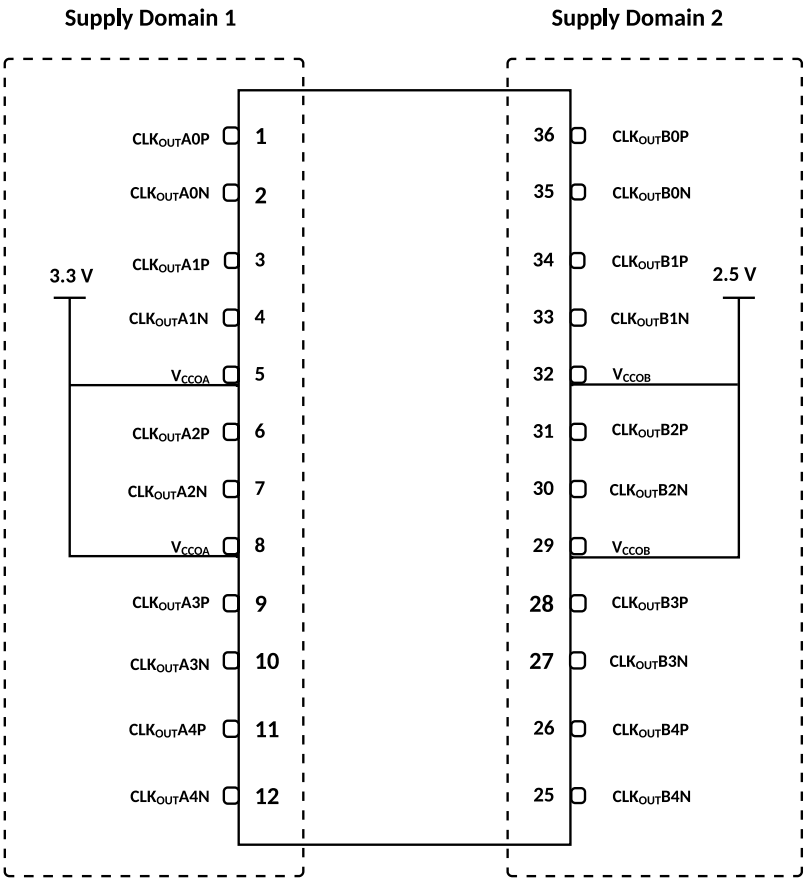
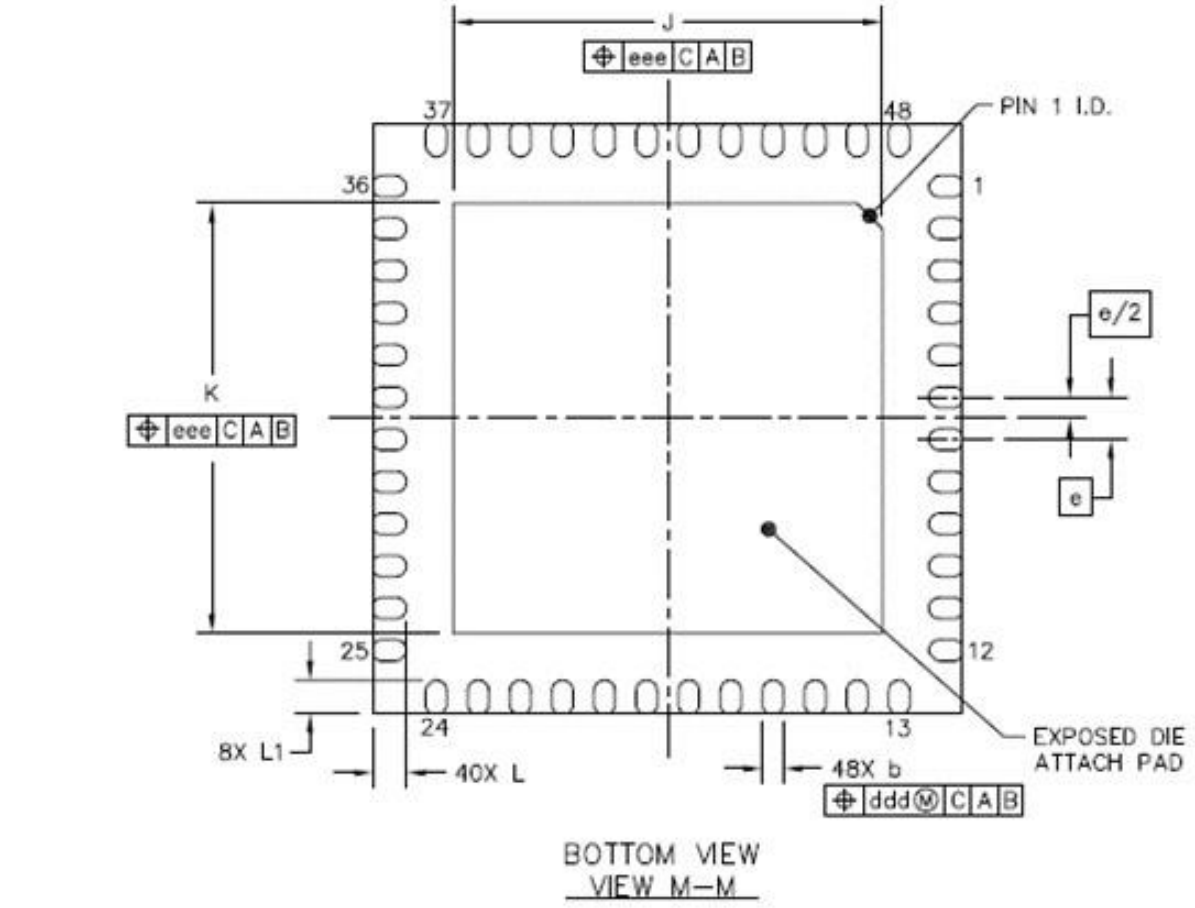


Figure 48: Multi Supply operation of AU5411

8 Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5	5.1	5.2
	Y	K	5	5.1	5.2
LEAD LENGTH		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 49 AU5411 48 pin, 7x7 QFN package dimensions

Notes:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.
- This drawing is subject to change without notice.
- The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

9 Ordering Information

Table 17 Ordering Information for AU5411

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temp. Range
AU5411A-QMR(1)	AU5411A	48 QFN 7 mm x 7 mm	Tape and Reel	-40 °C to 85 °C
AU5411A-QMT(1)	AU5411A	48 QFN 7mm x 7mm	Tray	-40 °C to 85 °C
AU5411A-EVB	—	—	Evaluation Board	—

Notes:
1.Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote tray ordering option.

10 Revision History

Table 18 Revision History

Version	Date	Description	Author
0.1	31 May 2018	AU5411 Datasheet First Draft	Aurasemi
0.2	11 Jan 2019	Removed '-' from part number Added foot notes where ever applicable Expanded input clock configurations Expanded output clock configurations Component values specified in application diagrams Added diagram for REFOUT enable and disable	Aurasemi
0.3	16 Jan 2019	Added VCCO voltage information for PSRR	Aurasemi
0.4	23 Jan 2019	Added hot swap recommendations	Aurasemi
0.5	28 Jan 2019	Added section on parameter definitions for more clarity on data sheet parameters	Aurasemi
0.6	20 Feb 2019	Added diagram for HCSL AC coupled output termination	Aurasemi
0.7	04 Apr 2019	Updated HCSL VOH/VOL limits	Aurasemi
0.8	05 May 2019	Updated figure 29 to add AU5411 in LVDS mode driving CML receiver	Aurasemi
0.9	2 Jun 2019	Updated the chip current data sheet limits to center them. LVPECL VOD lower limit changed to 475mV. Added clarification on VIH, VIL in single ended DC case	Aurasemi
0.91	5 Jun 2019	Removed 1.8V support on VCC, VCCOA, VCCOB Updated typical values of PSRR Updated typical values of rise/fall times across LVPECL, LVDS, HCSL Operation of AU5411 in multi supply domain scenario is added Updated output duty cycle of LVCMOS driver for 200MHz < Fin < 250 MHz to 40 to 60% Updated typical propagation delay across all output standards. Added crystal mode jitter	Aurasemi
0.92	10 Jul 2019	Upper limit of core current updated by 0.3mA Core switching current value stated at 2100 MHz Upper limit of HCSL, LVDS current updated by 1mA Typical values of PN noise floor updated to match with char data Max value of IN/OUT delay added as per char data LVCMOS specification changed to match requirement of 50 Ω driver Added Rs=0 in the application diagram and its description of LVCMOS Updated LVPECL AC input termination Changed Draft to Limited production release Updated upper limit of LVPECL swing. Updated ordering information Added more explanation to crystal swing in AC coupled mode	Aurasemi
0.93	7th Sept 2020	Ordering Information Table 16 Updated Datasheet Updated with Aura Latest Format	Aurasemi
0.94	25th Sept 2020	Updated the Missing Package Dimension Table in Section 8: Package Information	Aurasemi
1.0	5th July 2021	1.Table 16 changed to update the Ordering Part Number and Marking information. 2. Production Datasheet version 1p0 released.	Aurasemi

Version	Date	Description	Author
1.1	26th Nov 2021	1. Table 1: Pin Description, Pin 38 description updated 2. Fig 34 updated 3. Fig 39 and Fig 40 modified. 4. Typo correction in section 3.5 5. Version number updated to 1.1	Aurasemi
1.2	19th May 2022	1. Added the support for 1.8V V_{CCOA}, V_{CCOB} power supply for HCSL driver. 2. Table 9 added for Filtered Phase Jitter Parameters PCIe Common Clocked (CC) Architecture	Aurasemi

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